PREFACE:

Why do circuit board designers consider EMC?

Electromagnetic Interface (EMI) is a major problem in modern electronic circuits, circuit board designers will have to e the interference (to achieve electromagnetic compatibility (EMC)) to have the circuit board operating as

Circuit Design Consideration for EMC

- **1:** An overview of EMI and EMC
- **2:** Component selection and Circuit design techniques for EMC
- **3:** Printed circuit board layout techniques for EMC
- **4:** Conclusion and Discussion

1. An Overview of EMI and EMC

- 1.1. Terms Related to EMC
- 1.2. Elements of the Electromagnetic Environment
- 1.3. EMC cost

1.1. Terms Related to EMC

- **Electromagnetic Compatibility (EMC)** --- The capability of electrical and electronic system, equipments, and devices to operate in their intended electromagnetic environment within a defined margin of safety, and at design level or performance, without **suffering or causing** unacceptable degradation as a result of electromagnetic interface. (ANSI C64.14-1992)
- **Electromagnetic Interference (EMI)** --- EMI is the process by which disruptive electromagnetic energy is transmitted from one electronic device to another via radiated or conducted paths (or both).

  In common usage, the term refers particularly to RF signal. EMI can occur in the frequency range commonly identified as “anything greater than DC to daylight”.
- **Immunity** --- A relative measure of a device or a system’s capability to withstand EMI exposure while maintaining a predefined performance level.
- **Susceptibility** --- A relative measure of device or system’s propensity to be disrupted of damaged by EMI exposure to an incident field or signal. It is the lack of immunity.

1.2. Elements of the Electromagnetic Environment

A simple EMI model consists of three elements:

- **EMI source**

Clock Circuitry, MPU/MCUs, ESDs, Transmitters, Electromechanical Relays, Switching Powers, and Lighting etc..

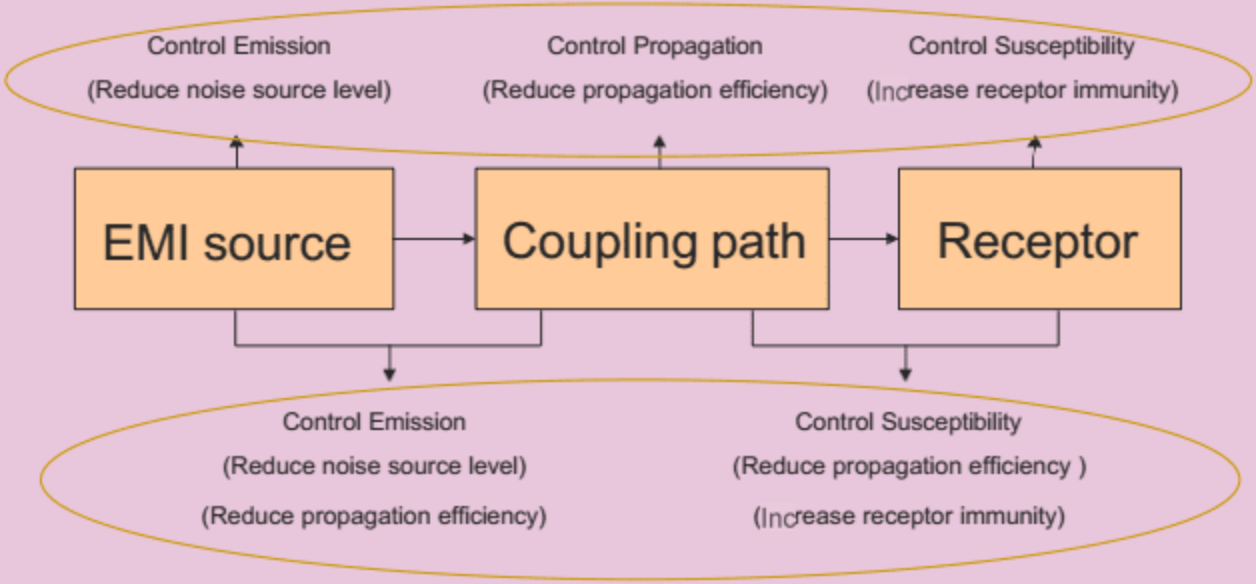
- **Coupling path**
  - ✓ **Conducted Path** : (Common) conductor,(parasitical) Capacitor, (parasitical) Inductor
  - ✓ **Radiated Path** : Radiated Electric and Magnetic Fields

- **Receptor**

All electronic circuits

1.2. Elements of the Electromagnetic Interference Environment (continued)

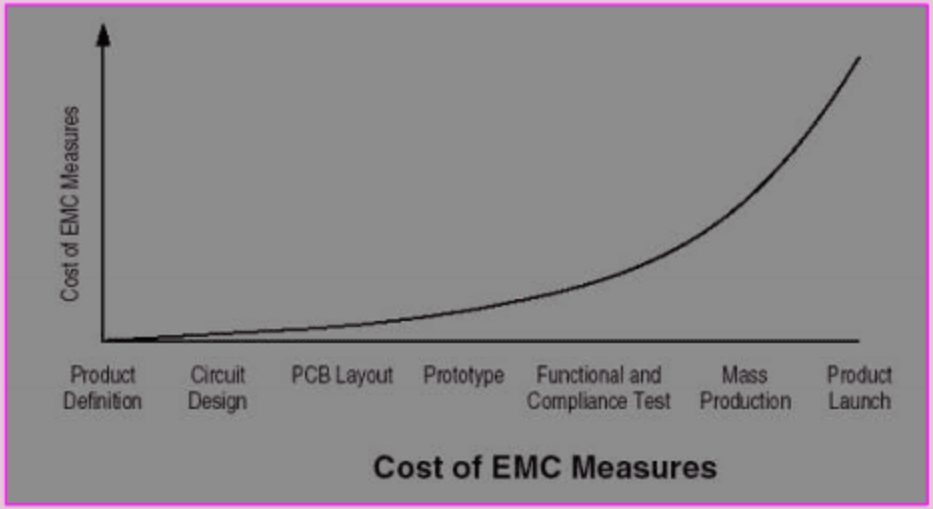
The simple EMI model is graphically in following figure.



EMI Elements

1.3. EMC Cost

The most cost-effective way to design for EMC is to consider the EMC at the early stages of the design. Cost of EMC measures is shown in following figure.



2. Component selection and Circuit design techniques for EMC

Component selection and circuit design are major factors that will affect board level EMC.

Each type of electronic components has its own characteristics, therefore requires careful design considerations.

- 2.1. Component Packages vs. EMC
- 2.2. Discrete Components Features vs. EMC
- 2.3. Integrated Circuits Features vs. EMC
- 2.4. Microcontroller/Microprocessor Circuits vs. EMC

2.1. Component Packages vs. EMC

Basic types :

- **Leaded**

Larger parasitic effects at high frequencies. The leads forms a low value inductor about 1nH/mm per lead and the end terminations can also produce a small capacitive effect in the region of 4pF.

- **Leadless**.

Less parasitic. Typically, 0.5 nH of parasitic inductance with a end termination capacitor of about 0.3pF.

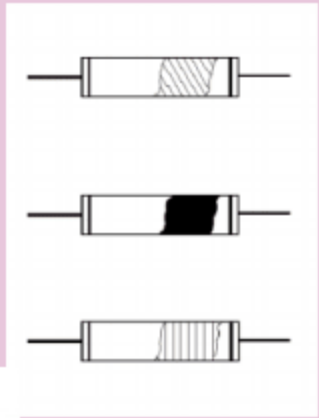
From an EMC viewpoint, surface mount components is preferred, followed by radial leaded, and then axial leaded.

2.2. Discrete Components Features vs. EMC

- 2.2.1. Resistors Features vs. EMC
- 2.2.2. Capacitors Features vs. EMC
- 2.2.3. Inductors Features vs. EMC
- 2.2.4. Diodes Features vs. EMC

2.2.1. Resistors Features vs. EMC

Surface mount resistor are always preferred over leaded types because of their low parasitic elements. For the leaded type, **from an EMC viewpoint,** the carbon film type is the preferred choice, followed by the metal film, then the wire wound.



2.2.2. Capacitors Features vs. EMC

Selecting right capacitor can solve many EMC problems because their function.

- ✓ 2.2.2.1. Types of capacitors
- ✓ 2.2.2.2. Bypass capacitors
- ✓ 2.2.2.3. Decoupling capacitors
- ✓ 2.2.2.4. Experience for capacitor using
- ✓ 2.2.2.5. Capacitors in schematics

2.2.2.1. Types of Capacitors

- **Aluminium electrolytic capacitor** are usually constructed by winding metal foil spirally and a thin layer of dielectric, which gives high capacitance per unit volume but increases internal inductance of the part.

- **Tantalum capacitors** are made from of the dielectric with direct plate and pin connections, which gives a lower internal inductance than aluminium electrolytic capacitors.

- **Ceramic capacitor** are constructed of multiple parallel metal plates within a ceramic dielectric. The dominant parasitics is the inductance of the plate structure and this usually dominates the impedance for most types in the lower MHz region.

- **Other capacitors**.

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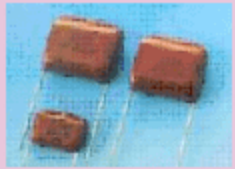


2.2.2.2. Bypass capacitors

The main function of the bypass capacitor is to create an AC shunt to remove undesirable energy from entering susceptible areas. It acts as a high frequency bypass source to reduce the transient circuit demand on the power supply unit.

Usually, the aluminium or tantalum capacitor is a good choice, its value depends on the transient current demand on the PCB and is usually in the range of 10 to 470uF. Larger value is required on PCBs with a large number of integrated circuits, fast switching circuits, and PSUs have long leads to the PCB.

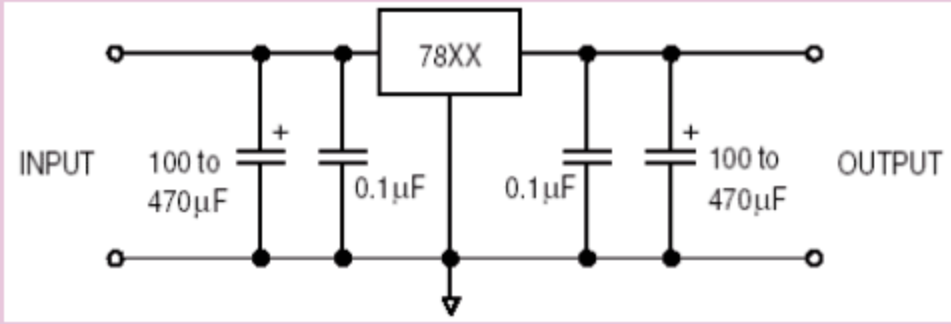
2.2.2.3. Decoupling capacitors

During active device switching, the high frequency switching noise created is distributed along the power supply lines. The main function of the decoupling capacitor is to provide a localized source of DC power for the active devices, thus decoupling the noise to ground to reduce the switching noise propagation across the board.

2.2.2.4. Experience for using capacitors

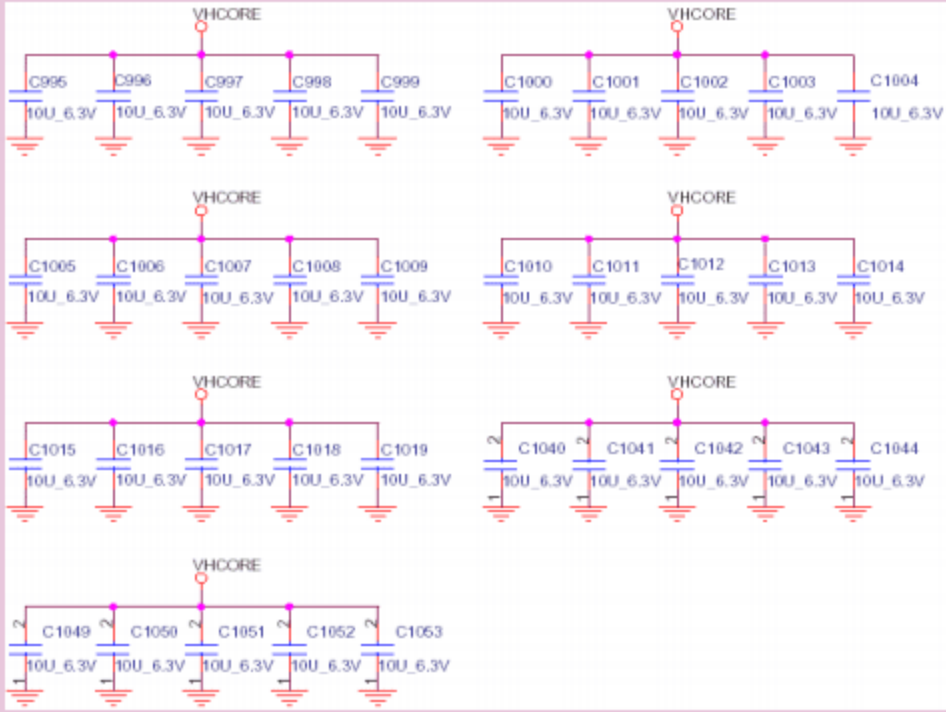
- Ideally, the bypass and decoupling capacitors should be placed as close as possible to the power supply inlet. The value of the decoupling capacitor is approximately 1/100 to 1/1000 of the bypass capacitor.
- For better EMC performance, decoupling capacitor should be placed as close as possibly to each IC, because track impedance will reduce the effectiveness of the decoupling. The value depends on the rise and fall time of the fastest signal. For example, with a 33MHz clock frequency, use 4.7nF to 100nF, with a 100MHz clock frequency, use 10nF.
- The ESR of the capacitor also affects its decoupling capability. It is preferable to choose capacitors with a ESR value below 1Ω.
- A common practice is to use two decoupling capacitors in parallel. This can provide a wider spectral distribution to reduce the switching noise induced by the power supply networks. Multiple decoupling capacitors connected in parallel can provide 6dB improvement to suppress RF currents generated by active device switching. The value of the two capacitors should differ by two orders of magnitude (e.g. 0.1uF+0.001uF connected in parallel).

2.2.2.5. Capacitor Examples



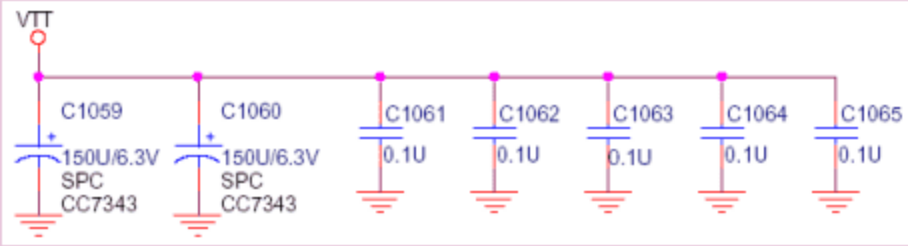
78XX Regulator

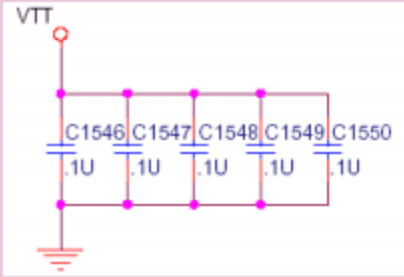
2.2.2.5. Capacitor Examples (Continued)



JM2 VHCORE (for CPU core)

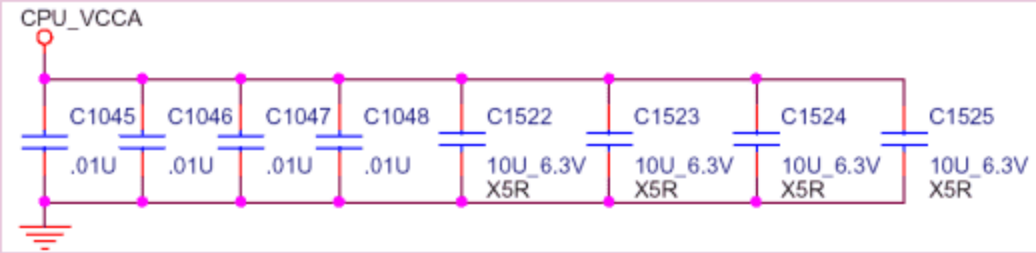
2.2.2.5. Capacitor Examples (Continued)





JM2 VTT (for CPU I/O port)

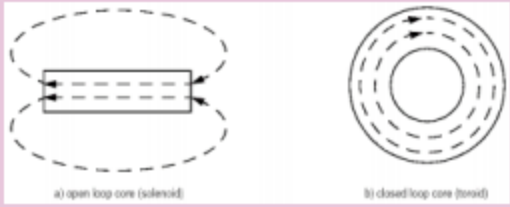
2.2.2.5. Capacitor Examples (Continued)



JM2 CPU_VCCA (for CPU core PLL)

2.2.3. Inductors Features vs. EMC

The inductors is the component which forms a link between magnetic and electric fields, hence are potentially more susceptible than other components as they have an inherent ability to interact with magnetic fields. Similar to capacitors, the inductor, when used intelligently, can provide a cure to many EMC problems.



open loop core vs. close loop core

rob inductor vs. bobbin inductor

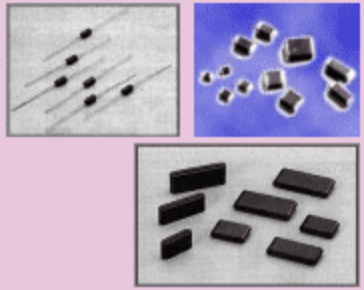
2.2.3. Inductors (continued)

Core material : iron and ferrite.

Iron core inductor are used for low frequency applications (tens of thousands) while ferrite core inductor is more suitable for EMC applications.

Two special types in EMC applications :
ferrite beads and ferrite clamps.

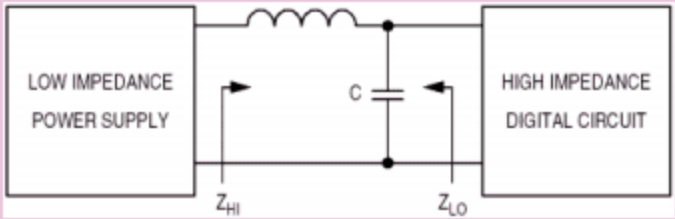
The ferrite bead is a single turn inductor and is usually a single lead through the ferrite. This device provides 10dB attenuation over the high frequency range and a low attenuation at DC. The ferrite clams provides 10 to 20 dB attenuation in both common (CM) and differential mode (DM) in the high Mhz region.



The inductor in DC-DC converter applications must have low emission and be able to handle high saturation currents, the bobbin shape inductor has these characters to fit this applications.

2.2.3. Inductors (continued)

In power supply application, a LC filter is needed to provided impedance matching between low impedance supply and high impedance digital circuit.

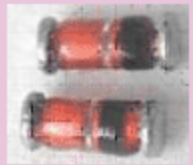


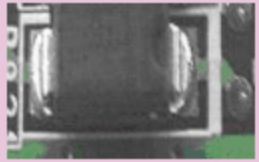
2.2.4. Diodes Features vs. EMC

The diode is the simple form of semiconductor devices. Based on their individual characters, some diodes can help to solve and protect from EMI related problems.

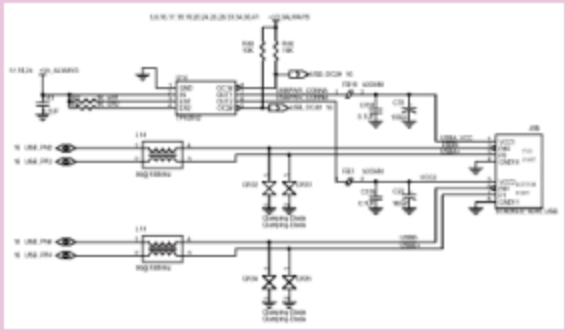
Diode Characteristics

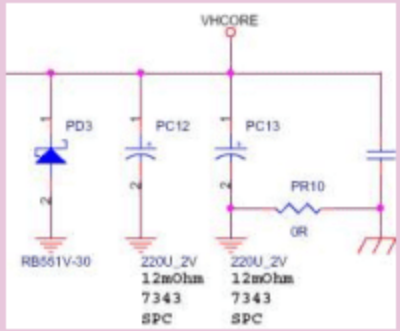
	Characteristic	EMC Application	Comments
Rectifier diode	Large current; slow response; low cost.	Nil	Power supply units.
Schottky diode	Low forward voltage drop; high current density; fast reverse transient time.	Fast transient signals and spike protection.	Switched mode power supplies.
Zener diode	Operation in reverse mode; quick reverse voltage transients; clamp positive transients only; tight clamp voltage	ESD protection; over voltage protection; low capacitance high data rate signalling protection.	—
Light emitting diode (LED)	Forward conduction mode; no EMC impact by itself.	Nil	Radiated emission when LED is mounted on a panel at a distance away from the PCB.
Transient voltage suppressor diode (TVS)	Similar to zener diode but in an avalanche mode; wide clamp voltage tolerance (e.g. 5V means clamp between 6V to 12V); clamp positive and negative voltage transients.	High voltage transient from ESD lighting – induced transient main spikes.	—
Varistor diode (VDR: voltage dependent resistor) (MOV: metal oxide varistor)	Metal coated ceramic pills (each pill works as schottky diode with high potential barrier; mains line protection; fastest response to transients.	First line ESD protection; high voltage and high transient protection.	Alternative to zener or TVS.

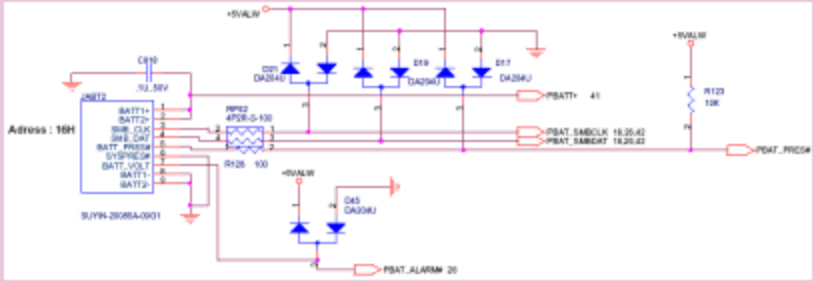




2.2.4. Diodes (continued)







2.3. Integrated Circuits Features vs. EMC

The majority of modern digital ICs are manufactured using CMOS technology. The static power consumption of CMOS devices may be lower, but with fast switching rates the CMOS device demands transient power from supply. The dynamic power demand of a high speed clocked CMOS device may exceed an equivalent bipolar device. Therefore, decoupling capacitors must be used on these devices to reduce the transient power demand from the power supply.

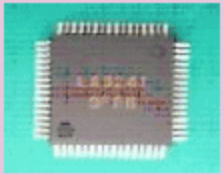
- 2.3.1. Integrated Circuit Package
- 2.3.2. Line Terminations

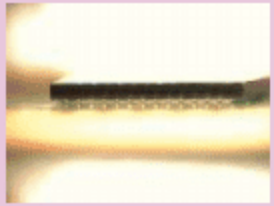
2.3.1. Integrated Circuit Package

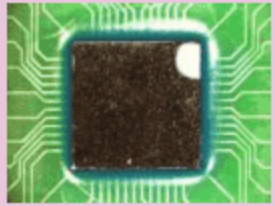
The shorter the lead, the less the EMI problem.

The surface mounts are preferred for better EMC performance because of lower package parasitics and smaller loop area. Further improvements are the use of die bonds, directly on the PCB.

The pins assignment of an IC can also affect EMC performance.





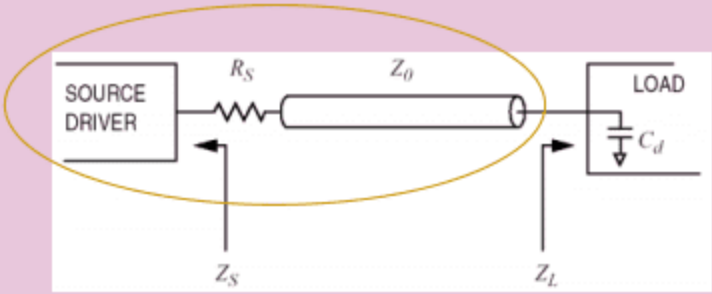


2.3.2. Line Terminations

When a circuit is operating at high speed, the impedance mismatching between the source and destination will cause signal reflection and ringing. The excess RF energy will also radiate or couple to other parts of the circuit. Termination of signal help to reduce these undesirable effects.

- ✓ 2.3.2.1. Series/Source termination
- ✓ 2.3.2.2. Parallel termination
- ✓ 2.3.2.3. RC termination
- ✓ 2.3.2.4. Thevenin termination
- ✓ 2.3.2.5. Diode termination
- ✓ 2.3.2.6. Summary of Termination

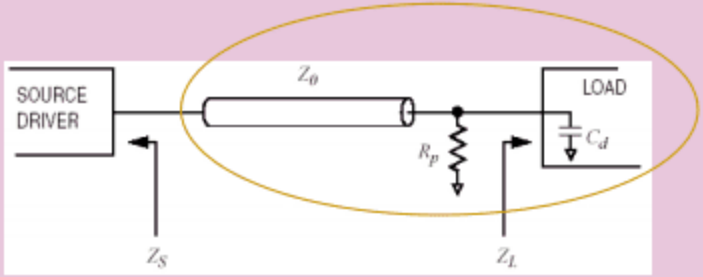
2.3.2.1. Series/Source termination



The source termination resistor, R_S is added to achieved impedance matching between the source, Z_S, and the distributed trace, Z_0. It can also absorb reflection from the load.

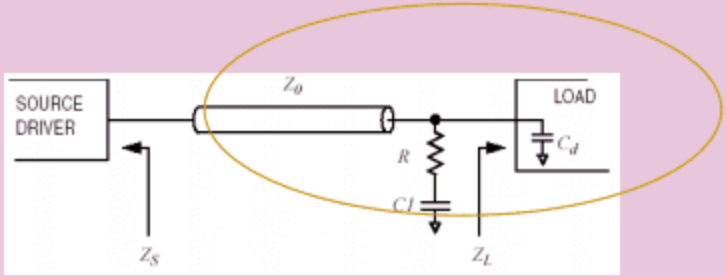
R_S must be placed as close as possible to the source driver. The value of R_S is the real part in the equation : $R_S = (Z_0 - Z_S)$. Typically, R_S equals to approximately 15 to 75Ω.

2.3.2.2. Parallel termination



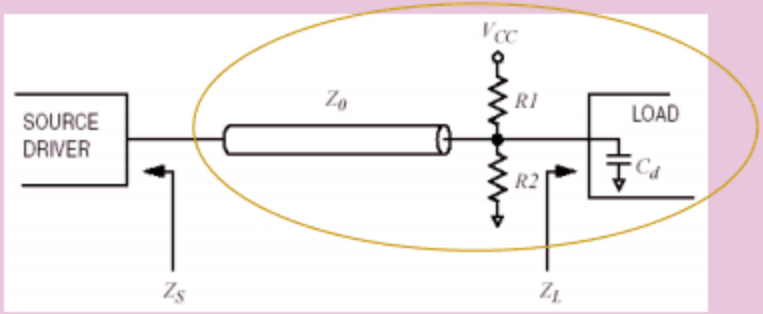
The parallel termination, R_p, is added, such that $R_p//Z_L$ is matched with Z0. But this method is not suitable for hand-held products, because of the low value of R_p (typically 50Ω), and will consume high power and requires the source driver to drive a high current. This method also adds a small delay by (Rp//ZL x Cd).

2.3.2.3. RC termination



The RC termination is similar to parallel termination, but with addition of Cl. The R provides impedance matching with Z_0, and C1 provides the drive current to drive the R and filter out the RF energy from the trace to ground. Therefore, the RC termination need less source driver current than the parallel termination. Value of R and C1 depends on Z_0, T_{pd} (round trip propagation delay), and Cd. Time constant, $RC=3xT_{pd}$, where $R//Z_L=Z_0$, $C=C1//C_d$.

2.3.2.4. Thevenin termination



The thevenin termination is formed by the R1 pull-up and R2 pull-down resistors, such that the logic high and low can meet the requirement of the destination load.

The value of R1 and R2 can be determined by R1//R2=Z_0.

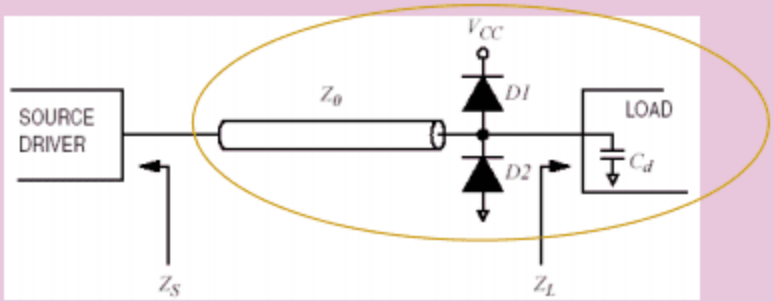
R1+R2+Z_L is such that the maxim current can not exceed the source driver capability.

For example, R1=220Ω, R2=330Ω

V_{ref}=R2/(R1+R2)xVCC=330/(330+220)x5=3V

Where VCC is the supply voltage.

2.3.2.5. Diode termination



The diode termination is similar to the thevenin termination, except that the resistors are replaced by diodes, which has a lower power consumption. The D1 and D2 configuration is used to limit overshoots of the reflected signal from the load. The diodes do not affect the line impedance, unlike the thevenin termination. Schottky and fast switching diodes are good choice for this type of termination.

The advantage of this termination is that Z_0 does not need to be known. This termination is commonly used inside MCUs for protection of I/O ports.

2.3.2.6. Line Terminations

Summary of Termination Methods

Termination Type	Relative Cost	Delay Added	Power Required	Critical Parameters	Characteristics
Series	Low	Yes	Low	$R_S = Z_0 = R_0$	Good DC noise margin
Parallel	Low	Small	High	$R = Z_0$	Power consumption is a problem
RC	Medium	Small	Medium	$R = Z_0$ $C = 20$ to 600pF	Check bandwidth and added capacitance
Thevenin	Medium	Small	High	$R = 2 \times Z_0$	High power for CMOS
Diode	High	Small	Low	—	Limits overshoot; some ringing at diodes

2.4. Microcontroller/Microprocessor Circuits Features vs. EMC

- 2.4.1. I/O port pins
- 2.4.2. Reset pin and IRQ pins
- 2.4.3. Oscillators

2.4.1. I/O port pins

With most MCUs and MPUs, input pins are usually high impedance.

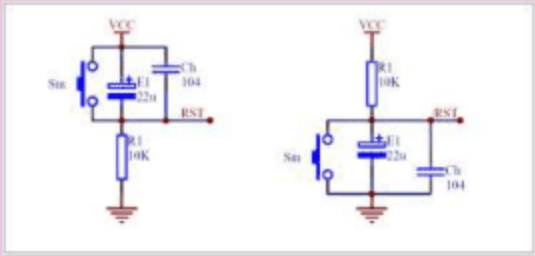
High impedance input pins are susceptible to noise and can register false levels if not properly terminated. When these pins are unconnected, they may result in a leakage and often float to the mid-point of the supply rail or to an undefined voltage.

Input pins which are not internally terminated need some high resistance (e.g. 4.7kΩ or 10kΩ) attached to each pin to ground or supply to ensure a known logic state.

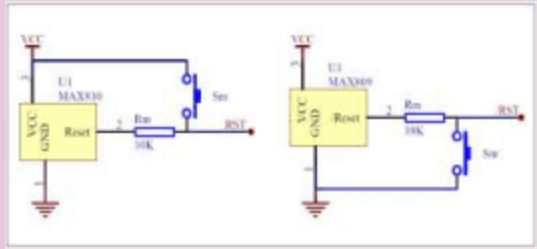
2.4.2. Reset pin and IRQ pins

The Reset and IRQ pins are the most important and critical pins of the MPU/MCU. If noise cause these pins to mis-trigger, a catastrophic effect will happen. For these pins, the termination is more important than the generate I/O port pins.

At power on, the supply rises to the mcu/mpu operating voltage, and there will be some time before it es stable. Therefore ,it is necessary to have some time delay on the reset pin. The delay circuit may be either RC (resistor-capacitor) network or RESET IC.

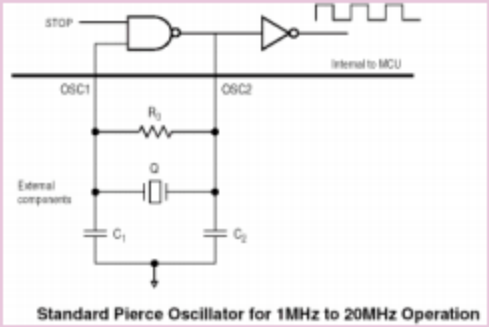


Basic RC reset circuits

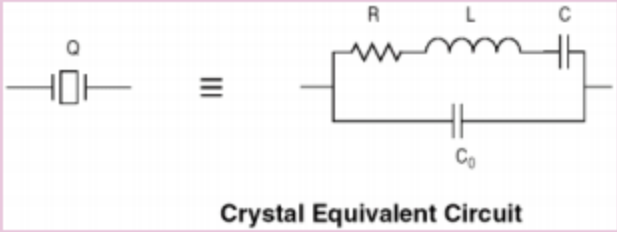


Reset IC reset circuits

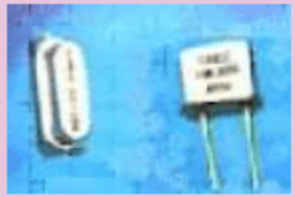
2.4.3. Oscillators



Standard Pierce Oscillator for 1MHz to 20MHz Operation



Crystal Equivalent Circuit



3. Printed circuit board layout techniques for EMC

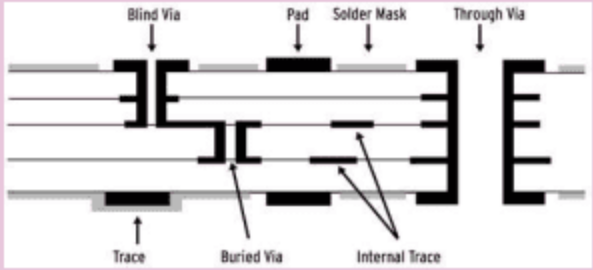
In addition to component selection and circuit design, good printed circuit board (PCB) design is an important factor in EMC performance. Since the PCB is an inherent part of the system, **EMC enhancements by PCB layout doesn't add extra cost towards the finish product**.

Most **PCB layout are restricted by board size and shape and the number of copper layers**. There are no fast and strict rulers for PCB layout. Much of it will depend on the experience of the PCB layout engineer.

3. Printed circuit board layout techniques for EMC

- 3.1. PCB Basic Characteristics
- 3.2. General guideline for PCB layout
- 3.3. Segmentation
- 3.4. Decouple Local Supplies and ICs
- 3.5. Trace Separation
- 3.6. Guard and Shunt Traces
- 3.7. Grounding Techniques
- 3.8. Tracking Layout Techniques

3.1. PCB Basic Characteristics



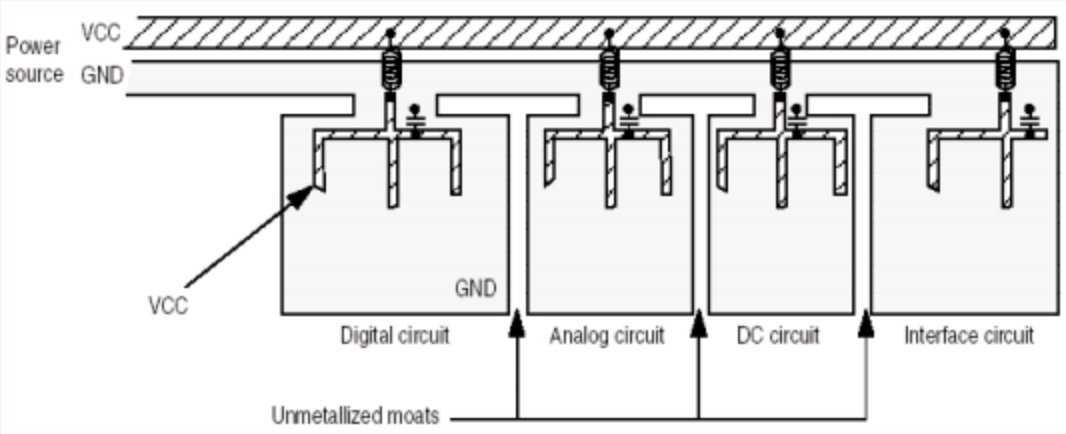
Track Characteristics:

- **Resistance** : The resistance of the track is determined by the weigh and cross-sectional area.
- **Capacitance** : The capacitance of the track is determined by the dielectric (*EoEr*), coverage area (*A*), an distance between tracks (*h*). The equation is C = *EoErA/h*.
- **inductance** : The inductance of the track is evenly distributed in the track. (approximately 1nH/mm

3.2. General guideline for PCB layout

- ✓ Increase the separation between tracks to minimize crosstalk by capacitive coupling.
- ✓ Maximize the PCB capacitance by placing the power and ground in parallel
- ✓ Place sensitive and high frequency tracks far away from high noise power tracks.
- ✓ Widen ground and power tracks to reduce the impedance of both power and ground.

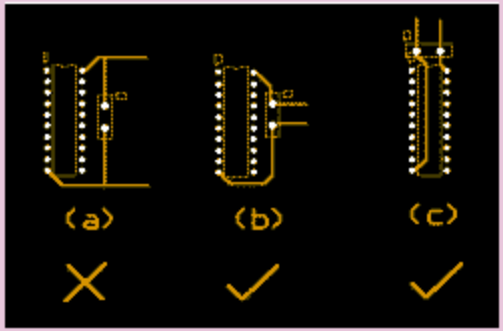
3.3. Segmentation



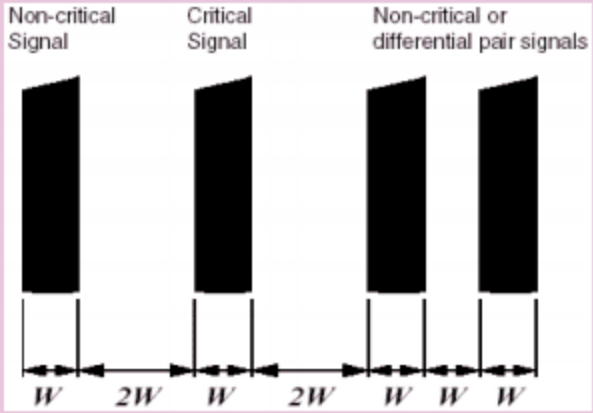
Segment is the use of physical separation to reduce the coupling between different types of circuit, particularly by the power and ground tracks.

3.4. Decouple Local Supplies and ICs

Localized decoupling can reduce noise propagating along the supply rail. Decoupling capacitors should be connected between power and ground at each IC, as close as possible to the pins. This helps to filter out switching noise from the IC.



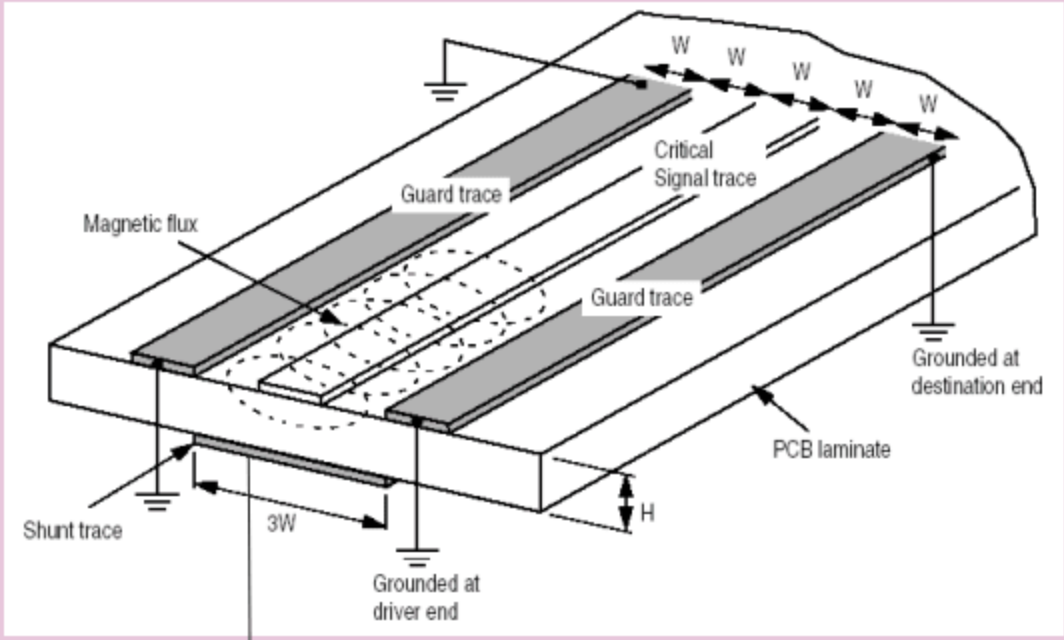
3.5. Trace Separation



3W Ruler

Trace separation is used to minimize the crosstalk and noise coupling (by magnetic flux coupling) between adjacent trace on the same PCB layer.

3.6. Guard and Shunt Traces



Doesn't need to be terminated (connected to ground)

3.7. Grounding Techniques

The objective of grounding technique is to **minimize the grounding impedance** and thus to reduce the potential of the ground loop from circuit back to the supply.

- 3.7.1. Ground track in single-layer PCBs
- 3.7.2. Ground track in double-layer PCBs
- 3.7.3. Guard ring
- 3.7.4. PCB capacitor
- 3.7.5. Fast circuits and slow circuits
- 3.7.6. Ground and power planes in multi-layer PCBs
- 3.7.7. Ground copper fills
- 3.7.8. Multi-power requirements

3.7.1. Ground track in single-layer PCBs
3.7.2. Ground track in double-layer PCBs

1. Ground track in single-layer PCBs

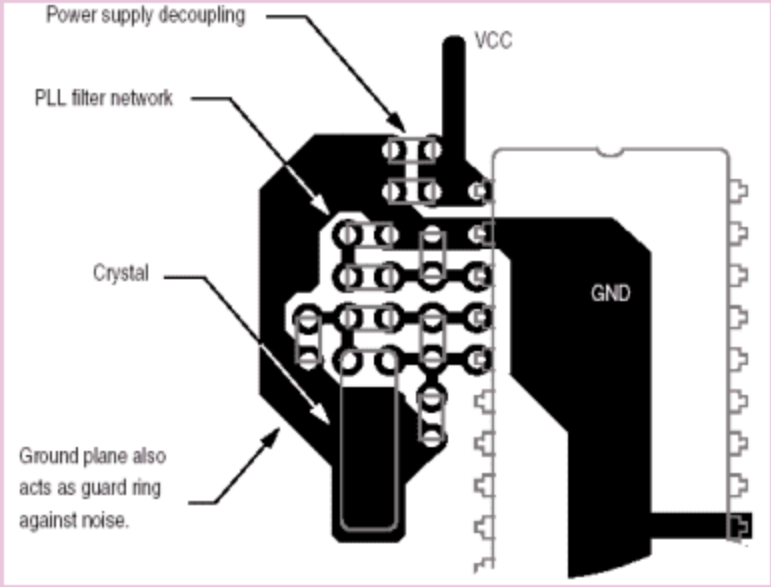
The width of the ground track should be as wide as possible. the use of jumper and changes in ground track width should be kept to a minimum, as these can cause change in impedance and inductance.

2. Ground track in double-layer PCBs

The ground grid/matrix arrangement is preferred for digital circuits because this arrangement can reduce ground impedance, ground loops, and signal return loops. As with single-layer PCBs, the width of the ground and power tracks should be as wide as possible.

Another scheme is to have a ground plane on one side, the signal and power on the other side. In this arrangement the ground return path and impedance will be further reduced and decoupling capacitor can be placed as close as possible between the IC supply line and the ground plane.

3.7.3. Guard Ring



The guard ring is a grounding technique that can isolate the noise (e.g. RF current) environment outside the ring.

3.7.4. PCB capacitor
3.7.5. Fast circuits and slow circuits

4. PCB capacitor

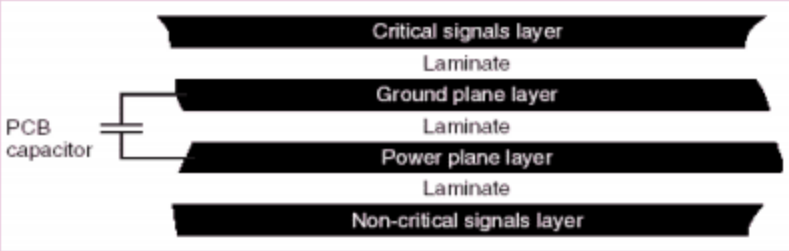
On a multi-layer board, a PCB is created by the thin laminate separating the power and ground planes. On a single-layer boars, this capacitor effect is also achieved by running the power and ground traces in parallel. The advantages of the PCB capacitor is that it has a very high frequency response and low series inductance that is evenly distributed decoupling capacitor on the whole board. No single discrete component has these characteristics.

5. Fast circuits and slow circuits

High speed circuits should be placed close to the ground plane while the slower circuits can be placed close to power plane.

3.7.6. Ground and power planes in multi-layer PCBs
3.7.7. Ground copper fills

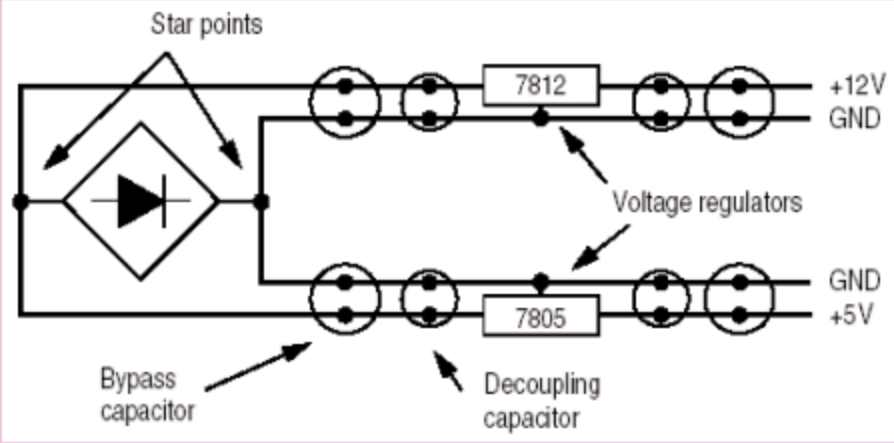
3.7.6. Ground and power planes in multi-layer PCBs



3.7.7. Ground copper fills

In some analog circuits, unused board areas are covered with a large **ground** such that it provides shielding and improve decoupling. But if the copper area is floating (e.g. not connected to ground), it may act as an antenna, and it will cause EMC problems.

3.7.8. Multi-power requirements



When the circuit requires more than one power supply, the idea is to keep each power separated by a ground plane. This help to avoid noise coupling from one power source to the other.

3.8. Tracking Layout Techniques

- 3.8.1. Vias
- 3.8.2. 45° angled tracking
- 3.8.3. Stubs
- 3.8.4. Star signal arrangement
- 3.8.5. Radiating signal arrangement
- 3.8.6. Constant track width
- 3.8.7. Hole and via concentrations
- 3.8.8. Split aperture
- 3.8.9. Ground metallized patterns
- 3.8.10. Minimize loop areas

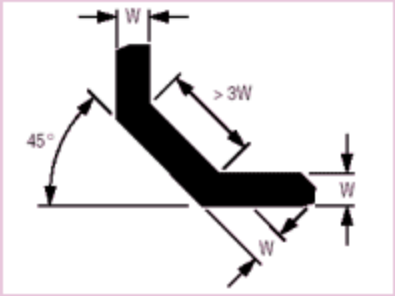
3.8.1. Vias
3.8.2. 45° angled tracking

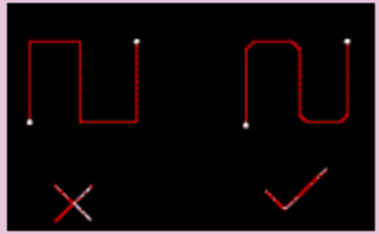
1. Vias

On a high speed signals, a via introduces 1 to 4nH of inductance and 0.3 to 0.8pF of capacitance to the track. Hence, vias should be kept to an absolute minimum. On high speed parallel lines (e.g. address and data lines), make sure the number of vias are the same on each signals line.

2. 45° angled tracking

Right-angle track turns should be avoid because noise that is produced at the inner edge can be couple to nearby tracks. Therefore, all orthogonal tracking should be 45° when making turns.

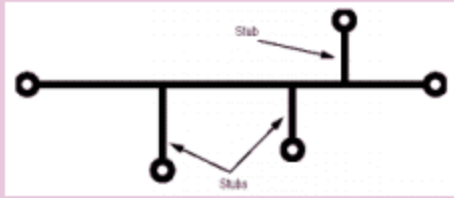




3.8.3. Stubs
4. Star signal arrangement
5. Radiating signal arrangement

- ## 3.8.3. Stubs

  Stubs produce reflections as well as the potential of adding wavelengh divisible aerials to the circuit.



- ## 3.8.4. Star signal arrangement

  The star arrangement should be avoid for high speed and sensitive signals because it introduce multiple stubs.

- ## 3.8.5. Radiating signal arrangement

  A radiating signal arrangement is usually the shortest tracking and causes minimum delay from source to all receivers, but this can cause multiple reflection and radiated interference. This should be avoided for high speed and sensitive signals.

3.8.6. Constant track width
3.8.7. Hole and via concentrations

- 3.8.6. Constant track width
- Varying track width creates changes in track impedance, this can cause reflections and line impedance imbalances.

- 3.8.7. Hole and via concentrations
- A concentration of via holes that pass through the power and ground planes produce a localized impedance difference near the holes. The area not only es a “hot spot” of signal activity, but the supply planes are high impedance at this point and less effective as RF sinks.

3.8.8. Split aperture
3.8.9. Ground metallized patterns

- ## 3.8.8. Split aperture

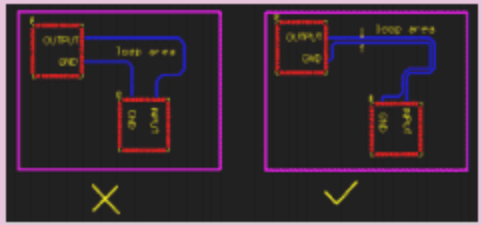
  This is same with hole and via concentrations, split apertures (i.e. log holes or wide vias) in power and ground planes create an area of non-uniformity and reduce their effectiveness as shields, as well as locally increasing the impedance of the power and ground planes.

- ## 3.8.9. Ground metallized patterns

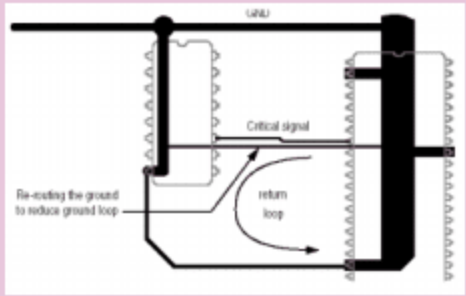
  All metallized patterns should be connected to ground, otherwise these large metal areas can act as radiating aerials.

3.8.10. Minimize loop areas

A current path is present from the load to the power supply source whether with ground plane or trace. The lower **the impedance of the return path** the better the EMC performance of the PCB. **The return path should be as short as possible, the loop area should be as small as possible.**



Keeping signal tracks and its ground return close together will help to minimize the ground loop. With high speed single-ended signals, sometimes the ground return may have to be tracked alongside the signal if the signal does not track over a low impedance ground plane.



4. Conclusion and Discussion

- 4.1. Conclusion
- 4.2. Discussion

4.1. Conclusion

The design consideration only discusses board level Designing consideration.

Although the circuit may be working at the board level, but it may be radiating noise to other parts of the system, causing problems at system level. Generally, only achieving board level EMC may not be enough. Further-more, EMC at the system or equipment level may have to satisfy certain emission standards, so that the equipment does not affect other equipment or appliances.

The PCB design rulers discussed are only ***general rulers***, they should be treated as ***general guideline***.

System Level EMC solution :

Shielding, Ground, (Power) Filter

4.2. Discussion

Discussion

THANK YOU !

EMC 的电路设计考虑电路兼容性设计-

NBDC，科技前沿

SG 领带修订版：1.1 批准人：JR Jen,W.L.Sung 2003.10.15

前言：

为什么电路板设计者要考虑 EMC?

电磁接口（EMI）是现代电子电路中的一个主要问题，电路板设计者必须消除干扰（以实现电磁兼容性（EMC），以使电路板正常工作）

EMC 的电路设计考虑

1：EMI 和 EMC 概述

2：EMC 的元件选择和电路设计技术

3：EMC 的印刷电路板布局技术

4：结论与讨论

1.EMI 和 EMC 概述

1.1.EMC 相关术语

1.2.电磁环境要素

1.3.EMC 成本

1.1.EMC 相关术语电磁兼容性 (EMC)-电气和电子系统、设备和装置在规定的安全裕度内、在设计水平或性能下在预期电磁环境中运行，而不会因电磁干扰而遭受或导致不可接受的退化的能力接口。(ANSI C64.14-1992)

电磁干扰 (EMI)-EMI 是破坏性电磁能量通过辐射或传导路径（或两者）从一个电子设备传输到另一个电子设备的过程。

在常见用法中，该术语特指 RF 信号。EMI 可能发生在通常被称为“大于直流到日光的任何频率”的频率范围内。

抗扰度 -设备或系统承受 EMI 暴露同时保持预定义性能水平的能力的相对度量。

敏感性 -设备或系统因暴露于事件场或信号的 EMI 而受到干扰或损坏的倾向的相对测量。它是缺乏免疫力。

1.2.电磁环境要素简单的 EMI 模型由三个要素组成：

电磁干扰源时钟电路、MPU/MCU、ESD、发射器、机电继电器、开关电源和照明等。

耦合路径传导路径：（公共）导体、（寄生）电容、（寄生）电感辐射路径：辐射电场和磁场受体所有电子电路

1.2.电磁干扰环境要素（续）

简单的 EMI 模型如下图所示。

控制发射控制敏感性（降低噪声源水平）（降低传播效率）（降低传播效率）（增加受体免疫力）

电磁干扰元件

1.3.EMC 成本最经济有效的 EMC 设计方法是在设计的早期阶段就考虑 EMC。EMC 措施的成本如下图所示。

2.EMC 的元件选择和电路设计技术元件选择和电路设计是影响板级 EMC 的主要因素。

每种类型的电子元件都有其自己的特点，因此需要精心设计考虑因素。

2.1.组件封装与 EMC

2.2.分立元件特性与 EMC

2.3.集成电路特性与 EMC

2.4.微控制器/微处理器电路与 EMC

2.1.组件封装与 EMC

基本类型：

含铅高频时寄生效应较大。引线形成每根引线约 1nH/mm 的低值电感器，并且终端还可产生 4pF 范围内的小电容效应。

无铅。

寄生较少。通常，寄生电感为 0.5 nH，末端电容约为 0.3pF。

从 EMC 角度来看，表面贴装元件是首选，其次是径向引线，然后是轴向引线。

2.2.分立元件特性与 EMC

2.2.1.电阻特性与 EMC

2.2.2.电容器特性与 EMC

2.2.3.电感器特性与 EMC

2.2.4.二极管特性与 EMC

2.2.1.电阻特性与 EMC

表面贴装电阻器总是优于引线型电阻器，因为它们的寄生元件较低。对于引线型电阻器，从 EMC 角度来看，碳膜型是首选，其次是金属膜型，然后是绕线型。

2.2.2.电容器特性与 EMC

选择正确的电容器可以解决许多 EMC 问题，因为它们的功能。

2.2.2.1.电容器的种类

2.2.2.2.旁路电容

2.2.2.3.去耦电容

2.2.2.4.电容器使用经验

2.2.2.5.原理图中的电容器

2.2.2.1.电容器的类型铝电解电容器有通常由螺旋状缠绕金属箔和一层薄薄的电介质构成，单位体积具有高电容，但增加了　　零件的电感。钽电容器是由电介质直接制成板和引脚连接，提供较低的　　电感比铝电解电容器。

陶瓷电容器由陶瓷电介质内的多个平行金属板构成。主要的寄生参数是板结构的电感，这通常在较低 MHz 区域的大多数类型中主导阻抗。

其他电容器。

2.2.2.2.旁路电容

2.2.2.3.去耦电容

2.2.2.2.旁路电容旁路电容器的主要功能是创建交流分流器，以消除进入敏感区域的不需要的能量。它充当高频旁路源，以减少对电源单元的瞬态电路需求。

通常，铝或钽电容是不错的选择，其值取决于 PCB 上的瞬态电流需求，通常在 10 至 470uF 范围内。在具有大量集成电路、快速开关的 PCB 上需要更大的值电路和 PSU 有很长的引线连接到 PCB。

2.2.2.3.去耦电容在有源器件开关过程中，产生的高频开关噪声沿着电源线分布。去耦电容的主要作用是为有源器件提供局部直流电源，从而将噪声去耦到地，以减少开关噪声。噪声全面传播。

2.2.2.4.电容器使用经验理想情况下，旁路和去耦电容应尽可能靠近电源入口放置。去耦电容的值约为旁路电容的 1/100 至 1/1000。

为了获得更好的 EMC 性能，去耦电容应尽可能靠近每个 IC 放置，因为走线阻抗会降低去耦的有效性。该值取决于最快信号的上升和下降时间。例如，使用 33MHz 时钟频率，使用 4.7nF 至 100nF，时钟频率为 100MHz，使用 10nF。

电容的 ESR 也影响其去耦能力，最好选择 ESR 值在 1Ω 以下的电容。

常见的做法是并联使用两个去耦电容。这可以提供更宽的频谱分布，以减少电源网络引起的开关噪声。并联多个去耦电容可以提供 6dB 的改善，以抑制有源器件开关产生的射频电流.两个电容的值应相差两个数量级（例如并联 0.1uF+0.001uF）。

2.2.2.5.电容器示例

78XX 调节器

2.2.2.5.电容器示例（续）

JM2 VHCORE（用于 CPU 核心）

2.2.2.5.电容器示例（续）

JM2 VTT（用于 CPU I/O 端口）

2.2.2.5.电容器示例（续）

JM2 CPU_VCCA（用于 CPU 核 PLL）

2.2.3.电感器特性与 EMC

电感器是在磁场和电场之间形成联系的组件，因此比其他组件更容易受到影响，因为它们具有与磁场相互作用的固有能力。与电容器类似，电感器在智能使用时可以提供解决方案许多 EMC 问题。

开环磁芯与闭环磁芯 Rob 电感器与骨架电感器

2.2.3.电感器（续）

磁芯材料：铁和铁氧体。铁芯电感器用于低频应用（数万次），而铁氧体磁芯电感器更适合 EMC 应用。

EMC 应用中的两种特殊类型：铁氧体磁珠和铁氧体夹。铁氧体磁珠是单匝电感器，通常是穿过铁氧体的单根引线。该器件在高电压下提供 10dB 衰减。

铁氧体蛤在高 Mhz 区域的共模（CM）和差模（DM）中提供 10 至 20 dB 的衰减。

DC-DC 转换器应用中的电感器必须具有低发射并能够处理高饱和电流，绕线管形状电感器具有这些特性来适合该应用。

2.2.3.电感器（续）

在电源应用中，需要一个 LC 滤波器来提供低阻抗电源和高阻抗数字电路之间的阻抗匹配。

2.2.4.二极管特性与 EMC

二极管是半导体器件的简单形式。根据其各自的特性，一些二极管可以帮助解决和防止 EMI 相关问题。

2.2.4.二极管（续）

2.3.集成电路特性与 EMC 大多数现代数字 IC 均采用 CMOS 技术制造。CMOS 器件的静态功耗可能较低，但由于开关速率较快，CMOS 器件需要来自电源的瞬态功率。高速时钟 CMOS 器件的动态功耗需求可能会超过等效双极器件。因此，这些器件上必须使用去耦电容器，以减少电源的瞬态功率需求。

2.3.1.集成电路封装

2.3.2.线路终端

2.3.1.集成电路封装引线越短，EMI 问题越少。

由于较低的封装寄生效应和较小的环路面积，表面贴装是获得更好 EMC 性能的首选。进一步的改进是直接在 PCB 上使用芯片接合。

IC 的引脚分配也会影响 EMC 性能。

2.3.2.线路终端当电路高速工作时，源和目的地之间的阻抗不匹配会导致信号反射和振铃。多余的射频能量也会辐射或耦合到电路的其他部分。信号终止有助于减少这些不良影响。

2.3.2.1.系列/源端接

2.3.2.2.并行终止

2.3.2.3.RC 终止

2.3.2.4.戴维南终止

2.3.2.5.二极管终端

2.3.2.6.终止概要

2.3.2.1.系列/源端接添加源端接电阻 RS 是为了实现源 ZS 和分布式走线 Z0 之间的阻抗匹配。它还可以吸收来自负载的反射。

RS 必须尽可能靠近源驱动器放置。RS 的值是方程中的实部：RS=(Z0-ZS)。通常，RS 等于大约 15 至 75Ω。

2.3.2.2.并行终止添加并联终端 Rp，使 Rp/ZL 与 Z0 匹配。但这种方法不适合手持式产品，因为 Rp 值较低（通常为 50Ω），并且会消耗较高的功率，并且需要该方法还增加了一个小的延迟 (Rp/ZL x Cd)。

2.3.2.3.RC 终止

RC 端接与并联端接类似，但增加了 C1。R 提供与 Z0 匹配的阻抗，C1 提供驱动电流来驱动 R 并滤除走线到地的 RF 能量。因此，RC 端接需要比并联终端更少的源驱动器电流。R 和 C1 的值取决于 Z0、Tpd（往返传播延迟）和 Cd。时间常数，RC=3xTpd，其中 R/ZL=Z0，C=C1/Cd。

2.3.2.4.戴维宁终止戴维南终端由 R1 上拉和 R2 下拉电阻组成，这样逻辑高和低可以满足目标负载的要求。

R1 和 R2 的值可以由 R1/R2=Z0 确定。R1+R2+ZL 使得最大电流不能超过源极驱动器的能力。

例如，R1=220Ω，R2=330Ω Vref=R2/(R1+R2)xVCC=330/(330+220)x5=3V 其中 VCC 是电源电压。

2.3.2.5.二极管终端二极管端接与戴维宁端接类似，只是电阻被二极管代替，功耗更低。D1 和 D2 配置用于限制来自负载的反射信号的过冲。二极管不影响线路阻抗，与戴维南端接不同。肖特基和快速开关二极管是此类端接的不错选择。

这种端接的优点是不需要知道 Z0。这种端接通常在 MCU 用于保护 I/O 端口。

2.3.2.6.线路终端

2.4.微控制器/微处理器电路特性与 EMC

2.4.1.I/O 口引脚

2.4.2.复位引脚和 IRQ 引脚 .2.4.3.振荡器

2.4.1.I/O 口引脚对于大多数 MCU 和 MPU，输入引脚通常为高电平高阻抗输入引脚容易受到噪声的影响，如果未正确端接，可能会记录错误电平。当这些引脚未连接时，它们可能会导致泄漏，并且经常浮动到电源轨的中点或未定义的电压。

未 端接的输入引脚需要将一些高电阻（例如 4.7kΩ 或 10kΩ）连接到每个引脚接地或电源，以确保已知的逻辑状态。

2.4.2.Reset 引脚和 IRQ 引脚

Reset 和 IRQ 引脚是 MPU/MCU 最重要、最关键的引脚。如果噪声导致这些引脚误触发，将会发生灾难性的影响。对于这些引脚，终止比生成 I/O 端口更重要引脚。上电时，电源上升到 MCU/MPU 的工作电压，需要一段时间才能稳定。因此，需要在复位引脚上有一定的延时。延时电路可以是 RC（电阻）-电容器）网络或复位 IC。

基本 RC 复位电路复位 IC 复位电路

2.4.3.振荡器

3.EMC 的印刷电路板布局技术除了元件选择和电路设计之外，良好的印刷电路板 (PCB)设计也是影响 EMC 性能的一个重要因素。由于 PCB 是系统的固有部分，因此通过 PCB 布局来增强 EMC 不会增加额外的完成成本产品。

大多数 PCB 布局都受到电路板尺寸和形状以及铜层数量的限制。PCB 布局没有快速且严格的规则。这在很大程度上取决于 PCB 布局工程师的经验。

3.EMC 的印刷电路板布局技术

3.1.PCB 基本特性

3.2.PCB 布局的一般指南 .3.3.分段

3.4.解耦本地电源和 IC

3.5.迹线分离

3.6.保护和分流走线

3.7.接地技术

3.8.跟踪布局技术

3.1.PCB 基本特性赛道特点：

阻力：轨道的阻力由重量和横截面积决定。

电容：走线的电容由电介质（EoEr）、覆盖面积（A）、走线间距（h）决定。计算公式为 C=EoErA/h。

电感：轨道的电感均匀分布在轨道中。（约 1nH/mm

3.2.PCB 布局的一般指南增加轨道之间的间距，以最大限度地减少电容耦合产生的串扰。

通过并联电源和接地来最大化 PCB 电容将敏感和高频轨道放置在远离高噪声电源轨道的位置。

加宽地线和电源走线以降低电源和地的阻抗。

3.3.细分分段是利用物理隔离来减少不同类型电路之间的耦合，特别是电源和接地走线之间的耦合。

3.4.解耦本地电源和 IC

局部去耦可以减少沿电源轨传播的噪声。去耦电容器应连接在每个 IC 的电源和地之间，并尽可能靠近引脚。这有助于滤除 IC 中的开关噪声。

3.5.迹线分离

3W 尺子走线分离用于最大限度地减少同一 PCB 层上相邻走线之间的串扰和噪声耦合（通过磁通量耦合）。

3.6. 保护和分流走线不需要端接（接地）

3.7. 接地技术接地技术的目的是最小化接地阻抗，从而降低从电路到电源的接地环路的电势。

3.7.1. 单层 PCB 中的接地线

3.7.2. 双层 PCB 中的接地线

3.7.3. 保护环

3.7.4. PCB 电容

3.7.5. 快速电路和慢速电路

3.7.6. 多层 PCB 中的接地层和电源层

3.7.7. 接地铜填充

3.7.8. 多电源要求

3.7.1. 单层 PCB 中的接地线

3.7.2. 双层 PCB 中的接地线

1.

单层 PCB 中的接地线地线的宽度应尽可能宽。跳线的使用和地线宽度的变化应保持在最低限度，因为这些可能会导致阻抗和电感的变化。

2.

双层 PCB 中的接地线数字电路首选接地网格/矩阵布置，因为这种布置可以减少接地阻抗、接地环路和信号返回环路。与单层 PCB 一样，地线和电源走线的宽度应尽可能宽。

另一种方案是一侧有接地层，另一侧有信号和电源。在这种布置中，接地返回路径和阻抗将进一步减少，并且去耦电容器可以尽可能靠近 IC 电源线和 IC 电源线之间放置。地平面。

3.7.3. 保护环保护环是一种接地技术，可以隔离环外的噪声（例如射频电流）环境。

3.7.4. PCB 电容

3.7.5. 快速电路和慢速电路

4.

PCB 电容在多层板上，PCB 是由分隔电源层和接地层的薄层压板创建的。在单层板上，这种电容器效应也是通过并行运行电源和接地走线来实现的。PCB 的优点电容的优点是它具有非常高的频率响应和低串联电感，是在整个板上均匀分布的去耦电容。没有任何单个分立元件具有这些特性。

5.

快速电路和慢速电路高速电路应放置在靠近接地层的位置，而较慢的电路可以放置在靠近电源层的位置。

3.7.6.多层 PCB 中的接地层和电源层

3.7.7.接地铜填充

3.7.6.多层 PCB 中的接地层和电源层

3.7.7.接地铜填充在一些模拟电路中，未使用的板区域被大面积地覆盖，以提供屏蔽并改善去耦。但如果铜区域是浮动的（例如未接地），则它可能充当天线，并且会导致 EMC 问题。

3.7.8.多电源要求当电路需要多个电源时，我们的想法是通过接地层将每个电源分开。这有助于避免从一个电源到另一个电源的噪声耦合。

3.8.跟踪布局技术

3.8.1.通孔 .3.8.2.45° 角跟踪 .3.8.3.存根

3.8.4.星号信号布置

3.8.5.辐射信号布置

3.8.6.恒定轨道宽度

3.8.7.孔和通孔浓度

3.8.8.分割光圈

3.8.9.接地金属化图案

3.8.10.最小化环路面积

3.8.1.过孔 3.8.2.45° 角度跟踪

1.过孔在高速信号上，过孔会向走线引入 1 至 4nH 的电感和 0.3 至 0.8pF 的电容。因此，过孔应保持在绝对最小值。在高速并行线（例如地址和数据线）上，使确保每条信号线上的过孔数量相同。

2. 45° 角度跟踪应避免直角轨道转弯，因为内边缘产生的噪声会耦合到附近的轨道。因此，转弯时所有正交轨道应为 45° 。

3.8.3.

存根

4.

星号信号排列

5.

辐射信号排列

3.8.3. 存根短截线会产生反射以及在电路中添加波长可分割天线的潜力。

3.8.4. 星号信号布置对于高速和敏感信号，应避免星形排列，因为它会引入多个短截线。

3.8.5. 辐射信号布置辐射信号布置通常是最短的跟踪，并导致从源到所有接收器的最小延迟，但这可能导致多重反射和辐射干扰。对于高速和敏感信号，应避免这种情况。

3.8.6. 恒定轨道宽度

3.8.7. 孔和通孔浓度

3.8.6. 恒定轨道宽度不同的走线宽度会导致走线阻抗发生变化，这可能会导致反射和线路阻抗不平衡。

3.8.7. 孔和通孔浓度穿过电源层和接地层的过孔集中，会在孔附近产生局部阻抗差异。该区域不仅是信号活动的“热点”，而且电源层在该点处具有高阻抗，因此效率较低射频接收器。

3.8.8. 分割光圈

3.8.9. 接地金属化图案

3.8.8. 分割光圈这与孔和过孔的集中度相同，电源和接地平面中的分割孔径（即圆孔或宽过孔）会产生不均匀区域并降低其作为屏蔽的有效性，并局部增加电源和接地的阻抗飞机。

3.8.9. 接地金属化图案所有金属化图案都应接地，否则这些大的金属区域可能会充当辐射天线。

3.8.10. 最小化环路面积从负载到电源，无论有接地层还是走线，都存在一条电流路径。返回路径的阻抗越低，PCB 的 EMC 性能越好。返回路径应尽可能短，环路面积应尽可能小。

保持信号走线及其接地回路靠近在一起将有助于最大限度地减少接地环路。对于高速单端信号，如果信号不在低阻抗接地层上跟踪，有时可能必须沿着信号跟踪接地回路。

四、结论与讨论

4.1.结论.4.2.讨论

4.1.结论设计考虑仅讨论板级设计考虑。虽然电路可能在板级工作，但它可能会向系统的其他部分辐射噪声，导致系统级问题。一般来说，仅实现板级 EMC 可能是不够的。此外，EMC 在系统上或者设备级别可能必须满足一定的排放标准，以便该设备不影响其他设备或器具。

所讨论的 PCB 设计标尺只是一般标尺，应将其视为一般准则。

系统级 EMC 解决方案：

屏蔽、接地、（电源）滤波器

4.2.讨论讨论