FPGA命名规则（FPGA naming rules）

The naming conventions for Altera are as follows:

Process + version + model +LE quantity + package + device speed.

Give an example:

EP2C20F484C6

EP process

2C cyclone2 (S stands for stratix. A stands for arria.)

20 2wLE quantity

F484 FBGA484pin package

C6 eight speed, the smaller the number, the faster the speed.

Well, first of all:

The amount of LE in the same device signal is more the better. At the same time, the more expensive

The number of pins in the same case is as good as possible.

The faster the device, the better.

FPGA may not be advanced, say: different products, different uses.

Cyclone series: a total of 3 generations of cyclone series, is FPGA's A version of the entry products. Covers a wide range, and the corresponding device, regardless of power consumption and speed are good. In small scale design, compete with Xilinx's spartan3A low-end market.

Stratix: a total of 4 generations of Stratix direct targeting large scale. High end markets such as digital signal processing and on chip systems. Both device speed and internal resources are entirely new architectures. As for chip systems and internal DSP, stratix4 and high-end Xilinx vertix5 become the mainstream of the top two companies in the high-end market.

ALTERA product model designation

XXX, XX, XX, X, XX, X, X

1234567

Process + model + LE quantity + package + pin number + temperature range + device speed.

1. prefix:

EP typical device

EPC composed of EPROM devices

EPF, FLEX, 10K or FLFX 6000 series, FLFX 8000 Series

EPM MAX5000 series, MAX7000 series, MAX9000 series

EPX flash logic device

2. device model

3.LE quantity: XX (k)

4. package form:

D ceramic dual in line

Q plastic quad flat package

P plastic dual in line

R Power Quad lead flat package

S plastic micro package

T thin type J lead chip carrier

J ceramic J shape lead chip carrier

W ceramic quad lead flat package

L plastic J shape lead chip carrier

B ball array

5. pin

6. temperature range:

C DEG C to 70 DEG c,

I -40, from 85 to,

M -55, from 125 to

7. speed:

The smaller the number, the faster the speed.

Give an example:

EP2C20F484C6

EP process

2C cyclone2 (S stands for stratix. A stands for arria.)

20 2wLE quantity

F484 FBGA484pin package

C6 eight speed

Xilinx company FPGA chip naming rules

For example, XC3S2000-5FGG676C

The XC3S is a SPARTAN family of device types

2000 is the 2 million system gate

-5 is high performance

The FGG676 is available in 676 pin FBGA packages

C is commercially available

What is the meaning of the commonly used CPLD/FPGA logo?

CPLD/FPGA manufacturers, more series, more varieties, each manufacturer naming and classification of different, to the application of CPLD/FPGA has brought some difficulties, but its logo is also a certain rule.

The following is a description of the commonly used CPLD/FPGA logos.

1) identification of CPLD/FPGA

CPLD/FPGA products can be divided into the following categories:

(1) for the manufacturer, such as: ALTERA, Lattice, Xilinx, is the company name.

(2) registered trademarks, such as: MAX is a registered trademark of the MAX series of CPLD products of ALTERA company.

(3) product model, such as EPM7128SLC84-15, is a CPLD (EPLD)

model of ALTERA company, which needs to be emphasized.

(4) product serial number, which is the serial number in the process of production, the sign of the product identity, and the identity card of the person.

(5) origin and other explanations. As multinational corporations operate internationally, the world is becoming increasingly globalized, and some products have indications of origin, such as made, in, China (made in China).

2) CPLD/FPGA product model logo composition

CPLD/FPGA product model identification is usually made up of the following sections:

(1) product line code: such as ALTERA's FLEX device series, the code is EPF.

(2) breed Code: for example, ALTERA's FLEX10K, 10K, is its breed code.

(3) characteristic code: that is, integration degree. CPLD products are usually described by logical macro units, and FPGA is usually described by efficient logic gates. As in ALTERA's EPF10K10, the latter 10 represents the typical product integration level of 10K. Be aware that the effective door is different from the available door.

(4) packaging code: such as LC in ALTERA's EPM7128SLC84, which means PLCC package (Plastic Leaded, Chip, Carrier, plastic

square flat package). PLD package except PLCC and BGA (Ball Grid Array C/JLCC (spherical mesh array), Ceramic /J-leaded Chip Carrier), C/M/P/TQFP (Ceramic/Metal/Plastic/Thin Quard Flat Package), PDIP/DIP (Plastic Double In line Package), PGA (Ceramic Pin Grid Array) as its acronym to describe, but should pay attention to the company slightly, such as PLCC, ATERA, LC, Xilinx, described by PC, Lattice, J used to describe.

(5) parameter description: for example, the LC84-15 in ALTERA's EPM7128SLC84, 84 represents 84 pins, and 15 represents the speed level of 15ns. But some products directly use system frequency to express speed, such as ispLSI1016-60, 60 represents maximum frequency 60MHz.

(6): general description of improved product design was improved in the follow-up, the improved design model in prototype number by letters, such as A, B, C etc. according to the sequence number, some from A, B, C according to the sequence number, it has a specific meaning, such as low D cost type (Down), E (Ehanced), enhanced L low power (Low), H (High), high pin type X extended type (eXtended) etc..

(7) the applicable environment: general description of levels in the model to describe the last letter, C (Commercial) said the commercial grade (0 degrees Celsius to 85 degrees Celsius), I (Industrial) said the industrial grade (-40 degrees Celsius to 100 degrees Celsius), M (Material) said the military grade (-55 degrees Celsius to 125 C).

3) several typical product models

(1) CPLD products and FPGA products of ALTERA company;

ALTERA's products typically begin with EP, which represents repeatable programming.

ALTERA company's MAX series CPLD products, series of code for EPM, typical product model meaning as follows:

EPM7128SLC84-15:MAX7000S series CPLD, the number of logic macrocell 128, using PLCC package, 84 pins, inter pin delay of 15ns.

ALTERA company's FPGA product family code is EP or EPF, the typical product model meaning is as follows:

EPF10K10:FLEX10K series FPGA, the typical logic size, is the 10K valid logic gate.

EPF10K30E:FLEX10KE series FPGA, logic scale is 3 times of EPF10K10.

EPF20K200E:APEX20KE series FPGA, logic scale is 20 times of EPF10K10.

EP1K30:ACEX1K series FPGA, logic scale is 3 times of EPF10K10.

EP1S30:STRATIX series FPGA, logic scale is 3 times of EPF10K10.

The FPGA configuration device series code of ALTERA company is EPC, and the typical product model has the following meanings:

EPC1: configure devices for type 1 FPGA.

(2) CPLD and FPGA device series of Xilinx company

Xilinx's products usually begin with XC, which represents the products of Xilinx company. Typical product models have the following meanings:

XC95108-7 PQ 160C:XC9500 series CPLD, logic macrocell number 108, between pin delay is 7ns, use PQFP package, 160 pins, commercial.

XC2064:XC2000 series FPGA, configurable logic blocks (configurable, Logic Block, CLB) to 64 (this model is characterized by CLB).

XC2018:XC2000 series FPGA, typical logic scale, is valid gate 1800.

XC3020:XC2000 series FPGA, typical logic scale, is valid gate 2000.

XC4002A:XC4000A series FPGA, the typical logic size, is the 2K valid gate.

XCS10:Spartan series FPGA, the typical logic scale is 10K.

XCS30:Spartan series FPGA, the typical logic scale is 3 times of XCS10.

(3) CPLD products of Lattice company

Lattice, CPLD, FPGA in the beginning of the products of the invention of the ISP, ispLSI, ispMACH series code, ispPAC and the new development of the ispXPGA, ispXPLD, wherein ispPAC is a programmable analog device, the following ispLSI, ispXPGA series of products were as follows:

IspLSI1016-60:ispLSI1000 series CPLD, universal logic block GLB number (only 1000 series as characteristic) for 16, the maximum operating frequency of 60MHz.

IspLSI1032E-125 LJ:ispLSI1000E series CPLD, universal logic block GLB number of 32 (quite logical macrocell number 128), maximum operating frequency 125MHz, PLCC84 package, low voltage commercial products.

IspLSI2032:ispLSI2000 series CPLD, logical macrocell 32.

IspLSI3256:ispLSI3000 series CPLD, logical macrocell 256.

IspLSI6192:ispLSI6000 series CPLD, logical macrocell 192.

IspLSI8840:ispLSI8000 series CPLD, logical macrocell 840.

IspXPGA1200: ispXPGA1200 series FPGA, the typical logical scale is the 1200k system gate.