EMC 仿真（EMC simulation）

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PCB simulation can be divided into a lot of kinds, with analysis of signal integrity (SI), electromagnetic compatibility (EMC) analysis, power integrity (PI), Thermal analysis (Thermal), contact more in current electronic product design is the first three, and SI and EMC problem seems to be more attention.

SI problems can be divided into distortion and delay distortion is mainly due to the reflection (impedance mismatch), crosstalk (capacitive or inductive coupling between signal), loss (loss of skin effect and the dielectric loss), and other causes. Delay is mainly related to signal transmission time, mainly depending on the length of the signal. The EMC problem mainly discusses the influence of electromagnetic radiation generated by current voltage variation in signal.

From the point of the design process, simulation and PCB can be divided into simulation before and after the simulation, the simulation is to point to in PCB Layout before take out sensitive within the circuit network, pre-built its topology structure, wiring parameters, the simulation to compare the different topology structure with linear parameter's influence on the signal transmission, and summarized a set of suitable design constraints (such as line width, line length, plate structure, etc.) to guide the Layout of actual work. After the design of PCB, the post-simulation is analyzed, and the wiring effect is

tested.

Software such as HyperLynx and Allegro SpecctraQuest can handle the problems of PCB's SI and EMC problems. The simulation step is similar, and set the laminar structure -- > select simulation network -- > adds model/set non-memory component parameters and circuit working frequency -- > runs simulation

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High speed circuit board (PCB) simulation

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Briefly describes the simulation process of printed circuit boards, the simulation for the importance of high quality, high precision PCB design, and on the PCB of scene generator using the simulation tool to key signal (the clock signal) for signal integrity and EMC analysis, and the string around the problem of parallel signal analysis, according to the simulation results to adjust the original design, so as to achieve the goal of improve the quality of the signal.

Key words: transmission line; IBIS model; Signal integrity; Electromagnetic compatibility

preface

In high-speed IC design, with the improvement of speed and

density of wiring system, signal integrity (SI), series wound, EMC problems for high quality PCB design more and more important, in the existing PCB up analysis and found that the problem is a very difficult thing, even if found the problem, for a completed PCB to implement effective solution also need to spend a lot of time and cost. At the beginning of the design and the design process, by contrast, is considering the impact of these aspects, modify the same question it takes much less time and money, so you need to seek a can in physical design prior to search, discover and eliminate or reduce these problems in the process of circuit design, according to the actual physical design of various parameters, in-depth and meticulous analysis method, the simulation is one of them.

There are two kinds of PCB simulation: line simulation and board level simulation. Line simulation can according to the requirement of the design of signal integrity and timing, help the designer to adjust before wiring components layout, programming the system clock network and determine the key line network termination strategy, track in the process of wiring design, any feedback wiring effect; In PCB board level simulation is usually carried out after completion of basic design, can be considered, such as electrical, EMC, thermal and mechanical properties, etc, the impact of these factors on the SI and mutual influence between these factors, thus the real system level analysis and validation, and line simulation, by contrast, is more complex. Before has not yet started wiring line simulation, known as the hypothetical simulation, the simulation to estimate the influence of all kinds of circuit elements, to

set parameters and wiring constraints, key network termination strategy to provide a certain basis.

The scene generator is a special plate for data processing. Its clock frequency is 33MHz and the signal speed is relatively fast.

Wiring density is bigger, to guarantee the normal work of the system, the design of the PCB must solve the problem of the signal integrity and EMC, this article, the authors use simulation techniques to estimate the signal integrity of the prediction is likely to cause, series wound and EMC problems, testing finished wiring transmission performance, comprehensive consider many sided, set reasonable wiring constraints, terminal matching strategy, etc.

2. Simulation process

Usually PCB simulation process is shown in figure 1, the first to establish the simulation model of components, then the hypothetical simulation to determine the wiring process need parameter Settings and some constraint conditions, the next in line at any time through the simulation in the process of actual wiring check wiring effect, finally carried out after completion of basic wiring board level simulation to check the performance of the system work.

Three simulation model

In the simulation process, the device needs to have the corresponding simulation model, and the accuracy of the

simulation model determines the accuracy of the simulation. IBIS and Spice models are commonly used. IBIS is used to describe the input, output, and I/O Buffer behavior characteristics of IC devices, and is used to simulate the interaction between the Buffer and the circuit system on the board. The core content in the IBIS model is the model of the Buffer, because these buffers generate some simulated waveforms that the emulator USES to simulate the impact of transmission lines. Because the IBIS describes the input and output impedance of Buffer, rising and falling time and in different situations and drop-down, engineers can use this model to simulate the system of the circuit on the PCB SI, crosstalk, EMC, and time series analysis. The IBIS model has a small amount of computation compared to the Spice model (usually only 1/10 to 1/100 of the corresponding Spice model), fast simulation speed, and no need to describe the I/O units

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Internal design and the transistor manufacturing parameters, the secrecy is strong, and is easy to be obtained from vendors, can carry on the accurate to the high-speed ringing and crosstalk fine simulation, considering the advantages of parasitic parameters of encapsulation, so for PCB simulation scene generator, device simulation model to choose the IBIS model.

The IBIS model can be searched from the manufacturer's website or generated by the editor. To build the IBIS model yourself, you first need to get the information necessary to build the model. These information includes components encapsulation type, tube leg number, the name of the tube legs and signal mapping relationship of the power supply voltage of the device size, components manufacturers, etc., with that information, the author use Hyplinx IBIS editor on scene generator all used to generate the corresponding device in the IBIS model, in the component library, ready for the back of the simulation.

Artificial simulation and line simulation

Before the hypothetical simulation, the location of large components on printed circuit board has been basically determined, as previously mentioned, at this time for later in the process of wiring signal which need terminal matching and how to use the terminal matching, as well as a variety of signal line width, line spacing parameters such as the set should be identified, due to the constraint conditions of these parameters are actually wiring, if the specified is unreasonable, may make the wiring quality is bad and even lead to the whole process of rework, for design staff, wasted a lot of time and energy,

The results are not satisfactory, therefore, hypothetical simulation is very important for PCB design.

From the design point of view, because of all the signal clock signal is usually chip work reference frequency, many

operations are on the basis of it, if the clock is not accurate, let alone chip worked, for this kind of the key signal integrity simulation's priorities should be. Below the author choose the scene generator in the representative of a set of the clock signal, hypothetical simulation, to determine which requires termination to the clock signal, choose what kind of terminal matching the most suitable.

Chips as shown in figure 2, A is A crystal, the 1, 2, 3 legs to chip B, D chip, chip C (33 MHZ) provide the same frequency clock as working clock chip, you can see that the location is closer to A, B, C, and D with A far distance, due to the differences in physical location, the clock driving end to distance at the receiving end, the clock line will have long have short, for long the clock line often need to pass through hole after the jump layer to reach the receiver, and also reflects the influence of the signal of this hole, some the clock line is very short, such as the clock line 1, the surface line, width of 8 mil (203 microns), its total length is only 306.97 mil (7.8 mm), some of the clock line is shorter, such as the clock line 3, from the surface through the hole to the middle line, width of 8 mil (203 microns), the total length of 826.98 mil (21 mm), and some clock line go distance is long, such as the clock line 2, the middle layer line, width of 10 mil (254 microns), among the total length of 3394.6 mil (86.2 mm). As is known to all, the signal transmitted from one end to the other end of the is need some time, electrical signal transmission speeds close to the speed of light can be thought of, therefore caused by propagation delay time for low speed digital circuit, clearly has little to do, but

for the high speed circuit has become a prominent problem, in fact, the rapid change of signal transmission in the long term, not only have the time delay, at the endpoint will produce reflection, waveform distortion, or noise pulse, lead to misoperation of the circuit. The ringing of a transmission line, overshoot, the effect increased with the increase of length of the line are becoming ever more obvious, therefore, for the length of the clock line should adopt corresponding measures to improve the transmission performance.

First we to the clock signal are simulated respectively, and the result waveform oscilloscope screen appears in the simulator, in figure 3 from the drive end 1 '1 and the receiving end of waveform can be seen, due to the drive end and receiving end itself apart is very close, connect their lead relatively flat, signal transmission distance is short, drive and basic waveform overlap at the receiving end, there is little distortion in signal in transmission process, so the clock without the source end or termination to get a better transmission performance. The waveform of the driver side 2 to the receiver 2 'can be clearly seen in the letter caused by the longer signal line

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Ringing effect, in this case, in fact, the clock signal is a high frequency noise in the system, the effect is close to its signal transmission quality, the resistor in series

with the source signal by one can eliminate the influence, in fact, due to the digital system has certain anti-interference capacity,

The transmission quality of this clock signal is generally considered acceptable.

But as the clock signal further extended, transmission quality will deteriorate further, drive on 3 '3' measured waveform and the receiving end, the two not only have differences in time, the shape difference is bigger also, the receiver on the measured signal voltage and a big overshoot and undershoot, its amplitude is very big, so that the receiver in each cycle will detect a redundant clock edge that we say normally off the clock, if the clock signal provided to chip, is likely to cause chip wrong operation, leading to chaos in the system the entire sequence, if this happens, the PCB design is a failure. The high frequency components in the waveform are also likely to be a very serious source of noise, affecting other signals. Therefore, we should give the clock signal with suitable terminal matching to improve the transmission characteristics of the clock signal, through the analysis and calculation, need to be in the receiver clock 3 'to add a parallel AC circuits, the resistance of 50 Ω, capacitance is 150 pf.

Now the clock signal that increases the terminal matching is resimulated. This time, the receiver port seems to be in a better waveform, as shown in figure in, most of the overshoot and undershoot are eliminated, drive is greatly

decreased and the signal at the receiving end shape differences, shows that the transmission quality is to promote, in fact, by increasing the capacitance value can be further coordinated waveform to eliminate all the overshoot.

Through the above analysis, we conclude that the length of the signal lines there is a big difference to the quality of transmission, the transmission quality variation with the length increase of line, for a long line, need to increase the source end or terminal match should be used to improve the quality of signal transmission.

Scene generator, the wiring density is bigger, a lot of signal lines inevitably need parallel wiring, and with the distance between line and line, the electromagnetic interference between each other and the coupling degree of intensity increased, line string around the problem is more and more prominent, string may cause false around the clock, intermittent data errors, etc., affect adjacent signals transmission quality, in fact, we don't need to completely eliminate strung around, as long as its control within the range of system are achieved. Produced by the principle of series wound can know, shorten the parallel line length, increase the distance between line and line, change the line width, reduce the dielectric constant, by changing the thickness of the lines to reduce the thickness of the dielectric, the change in the position of the interlayer can reduce the strength of the series wound.

Below we to scene generator of three parallel line (as

shown in figure 4), for example, in which drive the receiver of A and A ’between the transmission line called Aggressor# 1, B to B’ as the Victim, C to C ’for Aggressor# 2, in order to more clearly reflect the influence of series wound, the author through the drive end A and C to transmission line output the same signals (such as A rising edge), and the driver side B no signal output, keep A kind of static, no any signal to the Victim if no string around the influence, at the receiving end B’ should be less than any signal measurement, however, from the figure 5 shows that in the B ’in the existence of the received signal waveform measurement, the signal is A transmission line Aggressor# 1 and 2 to Victim at the static Aggressor# series wound caused by the waveform. If there is a data signal transmission on the Victim, the string is stacked up to the original signal, which is likely to cause intermittent data errors. In order to reduce the influence of series wound, we will line spacing increased from 8 mil (203 microns) to 12 mil (305 microns), and reduce the signal wire and coating the distance of the plane (from the original 10 mil (254 microns) reduce to 5 mil 127 mu (m)) and the simulation again these signals, waveform as shown in figure 5, it can be seen that signal the string around the Victim was greatly decreased.

From the Angle of signal integrity and string winding, the simulation and adjustment of the signal in the time domain is usually taken from the electromagnetic compatibility (EMC).

In the frequency domain, the signal is simulated and the

radiation intensity is reduced to reduce the electromagnetic radiation

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The purpose of interference.

Similarly, we still use the key network in the scene generator (clock signal 3) as an example to simulate the electromagnetic interference intensity before and after the increase of the terminal matching. No terminal matching were on clock signal line 3, the simulation results as shown in figure 6 (the length of the vertical bars show a signal at a frequency of electromagnetic radiation intensity, two horizontal lines is the radiation levels of government restrictions), can be seen clearly, signal generated by the noise from 0 hz to 1 GHZ, range is very wide, signal radiation intensity of each frequency point is not the same, there are some frequency points on the radiation intensity are beyond the government restrictions, which means that the signal of electromagnetic interference on this point has been beyond the degree of system can bear, in this case, should take measures to reduce the radiation levels. Here, we give the clock line with AC terminals as described above, simulation again, noted that more than government limit the frequency of the wave has been reduced to below the government, and the radiation intensity of each frequency point, the signal of the entire radiation

intensity decreased. This shows that for the long-term transmission signal, increasing the appropriate network of terminal matching not only improves the transmission characteristics of the signal, but also reduces the radiation level of the signal and improves the quality of the signal.

5 board level simulation

When the signal line, after the completion of the basic on the PCB before the formal cast version to PCB manufacturer, usually adopt board level simulation to check of the whole system, as well as the line simulation, the simulation results show that the signal integrity in the oscilloscope, EMC analysis results show that in the spectrum analyzer.

Line simulation is a design early a good way to solve the problem of signal integrity and EMC, at board level simulation to see many of the problems in fact online simulation can be solved, for instance, the clock signal terminal design is not correct. However, there are a lot of problems can only be found in the wiring is completed, even if the signal is designed right, but the impact is likely to be other signal adjustment, perhaps the line length is not strict limit within the wiring specification, may signal between the layers of jump too many times, and so on. These effects are difficult to predict before the actual wiring is completed, and it is the purpose of the board level simulation to find and solve these problems.

Here we use board level simulation on the finished scene

generator series wound analysis, and to analyze series wound, makes the simulation more effective, as far as possible choose those has obvious effects of the victim signal as the aggressors. Usually caused by victim recent wire series wound is larger, but sometimes a fast driver can make to the remote signal as the biggest aggressor, for tens of thousands of scene generator PCB line, hope that through simulation on every single way to look for the biggest aggressor, it is almost impossible. Hyplinx's Boardsim offers two ways to deal with this problem, the first is a series of intensity reports, which quickly estimate the intensity of each signal on the board. The second method is detailed Batch - Mode simulation.

In this case, a large number of signals to be emulated are queued up and run in the batch fashion, and the results appear in the report file. In our scene generator board level strung around in the simulation, using the first approach, because of series wound strength report provided by the data signal as the aggressors and the victim of how will play a strong guiding role, through its know need to for details see what signals, to take further measures to improve the performance of the signal. After confirmed the aggressors and victim, simulation of the process same as the above line simulation string around the process.

6 the conclusion

With the gradual improvement of the switching speed of digital devices, signal integrity, series winding and EMC analysis are more and more important for the design of high

speed PCB design. During the design period, signal integrity is carried out, and the problem of string and EMC analysis is beneficial to the constraints of PCB wiring. Avoid expensive PCB rework, saving a lot of time; Ensure that the delayed budget is met; Produce high-quality printed boards; Avoid tedious and costly test errors. In this paper, the simulation technology is used in the PCB design of the scene generator