fpga警告消除（FPGA warning elimination）

1、在“寄存器”<“>”时，在活动时钟边缘发现时钟敏感的变化

原因：矢量源文件中时钟敏感信号（如：数据，允许端，清零，同步加载等）在时钟的边缘同时变化。而时钟敏感信号是不能在时钟边沿变化的。其后果为导致结果不正确。

措施：编辑矢量源文件

2、Verilog HDL 分配警告，位置>截断值与大小> <数字>匹配目标的大小（<数字>

原因：在 HDL 设计中对目标的位数进行了设定，如：reg [4:0]一；而默认为 32 位，将位数裁定到合适的大小

措施：如果结果正确，无须加以修正，如果不想看到这个警告，可以改变设定的位数

3。所有到达作业 data_out（10）为“0”，登记被优化

原因：经过综合器优化后，输出端口已经不起作用了

4。以下 9 个引脚没有 GND 或 VCC，驱动数据端口，这个连接的变化可能改变拟合结果

原因：第 9 脚，空或接地或接上了电源

措施：有时候定义了输出端口，但输出端直接赋’0’，便会被接地，赋 1”接电源如果你的设计中这些端口就是这样用的，那便可以不理会这些警告。

5。发现引脚作为定义的时钟和/或记忆使

原因：是你作为时钟的引脚没有约束信息。可以对相应的引脚做一下设定就行了。主要是指你的某些管脚在电路当中起到了时钟管脚的作用，比如触发器的 CLK 管脚，而此管脚没有时钟约束，因此 QuartusII 把“时钟”作为未定义的时钟。

措施：如果 CLK 不是时钟，可以加“时钟”的约束；如果是，可以在时钟设置当中加入；在某些对时钟要求不很高的情况下，可以忽略此警告或在这里修改：作业>定时分析设置>个人>时钟……

6。设备 EPM570T144C5 时序特点初探

原因：因为 MAXII 是比较新的元件在 QuartusII 中的時序并不是正式版的，要等服务包

措施：只影响 Quartus 的波形

7：警告：当前设备家族支持 PLL 偏移的时钟延迟分析，但未启用

更多的时间——>

措施：将设置中的时序要求和选项-->设置-->设置使时钟延迟中的改成关上

器|

8。发现时钟的时候违反在 14.8 ns 的登记”|计数 lpm_counter：count1_rtl_0 | DFFS [11]”

看波形设置是否和

原因：违反了设置/保持时间，应该是后仿真，看时钟沿符合设置/保持时间

措施：在中间加个寄存器可能可以解决问题

9.warning：电路可能不 operate.detected 46 非操作路径的时钟偏移大于数据延迟时钟 clk44 时钟

原因：时钟抖动大于数据延时，当时钟很快，而如果等类的层次过多就会出现这种问题，但这个问题多是在器件的最高频率中才会出现

措施：设置-->选项-->需要定时要求和改小一些违约，如改到 50mhz

10。设计包含<号码>输入引脚（S）不驱动逻辑

原因：输入引脚没有驱动逻辑（驱动其他引脚），所有的输入引脚需要有输入逻辑

措施：如果这种情况是故意的，无须理会，如果非故意，输入逻辑驱动。

11。警告：发现时钟的时候违反了在节点上试验 8.9ns 时钟”。

原因：FF 中输入的请的保持时间过短

措施：在 FF 中设置较高的时钟频率

12 警告：在时钟路径中发现 10 个节点，它们可能充当纹波和/或门控时钟——节点被分析为缓冲器，导致时钟歪斜。

Reason: if you use CPLD with only one set of global clocks, another clock produced by dividing the global clock is used as a signal processing in the wiring, which cannot guarantee low clock skew (SKEW). The clock circuitry that

causes work on this clock is unreliable, and even wiring problems are different.

Measure: if you have FPGA chips with more than two sets of global clocks, you can solve the problem by using second global clocks as another clock.

13.Critical, Warning:, Timing, requirements, were, not, met., See, Report,, window, for, details.

Reason: timing requirements are not met,

Double click the Compilation Report-->Time Analyzer--> measures: the red part (such as clock setup:'clk'etc.) - > left click to view the Fmax SLACK path list, REPORT according to the prompt solution, there may be a problem of algorithm program

14.Can't, achieve, minimum, setup, and, requirement, <text>, along, <number>, path (s). See, Report, window, for, hold, details.

Reason: time series analysis finds that a certain number of paths violate the minimum set up and hold times, and are related to clock skew, usually caused by multiple clocks

Using Compilation Report-->Time Analyzer--> measures: the red part (such as clock, hold:'clk') in slack hold time observation is negative for setup or time is negative, then the increase in Editor-->To Assignment-->Assignment: clock name (from node finder), Assignment increased in Name

The Multicycle and Multicycle Hold options associated with multiple clocks, such as hold time, are negative, allowing the value of Multicycle hold to be >multicycle, such as 2 and 1.

15:, Can't, analyze, file -- file E://quartusii/*/*.v is missing

Reason: trying to compile a file that does not exist. The file may have been renamed or deleted

Measures: no matter what he does, it doesn't matter

16.Warning:, Can't, find, signal, in, vector, source, file, for,, input, pin, |whole|clk10m

Reason: because your file source (vector) doesn't add all the input signals (input, pin), you need an incentive source for each input

17.Error: Can't, name, logic, function, scfifo0, of, instance, Inst, function has, same, name, as,, current, design, file

The reason: the name of the module and project the name of the same name.

Measure: change one of the two names, and change the name of the module

18.Warning: Using design file lpm_fifo0.v, which is not specified as a design file for the current project, but contains definitions for 1 design units and 1 entities in project Info: Found entity 1: lpm_fifo0

Reason: the module is not generated in this project, but is generated directly from the schematic and source of the other project, rather than adding the file to the project using QUARTUS. Copy

Measures: do not bother, does not affect the use

19.Timing, characteristics, of, device, <name>, are, preliminary

Reason: the current version of QuartusII only provides preliminary timing characterization of the device

Measures: if you insist on using the current device, do not heed the warning. Further analysis of timing features will be complete in subsequent versions of Quartus.

20.Timing, Analysis, does, not, support, analysis, of, latches, as, synchronous, elements, the, for, the,, currently, selected, device, family

Reason: using analyze_latches_as_synchronous_elements setting allows Quaruts II to analyze synchronous latch, but the current device does not support this feature

Measures: no need to pay attention to. The timing analysis

may analyze the latch into loops. But it doesn't necessarily make sense. The consequences may cause the display to alert the user: change the design to eliminate the latch

21.Warning:Found, XX, output, pins, without, output, pin, load, capacitance, assignment, gucheng82

Reason: no specified load capacitance for output instruction

Measure: this feature is used to estimate TCO and power dissipation, and can also be used to specify the load capacitance for the corresponding output pins in the Assignment Editor to eliminate warnings

Twenty-two

警告：在时钟路径中发现 6 个节点，它们可能充当纹波和/或门控时钟——作为缓冲区分析的节点（s）导致时钟偏移。

原因：使用了行波时钟或门控时钟，把触发器的输出当时钟用就会报行波时钟，将组合逻辑的输出当时钟用就会报门控时钟

措施：不要把触发器的输出当时钟，不要将组合逻辑的输出当时钟，如果本身如此设计，则无须理会该警告

23。警告（10268）：Verilog HDL 的信息在 lcd7106。V（63）：总是构建包含阻塞与非阻塞赋值

原因：一个总是模块中同时有阻塞和非阻塞的赋值

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原因：矢量源文件中时钟敏感信号（如：数据，允许端，清零，同步加载等在时钟的边缘同时变化而时钟敏感信号是）。

不能在时钟边沿变化的。其后果为导致结果不正确。

措施：编辑矢量源文件

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原因：在 HDL 设计中对目标的位数进行了设定，如：reg [4:0]一；而默认为 32 位，将位数裁定到合适的大小

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原因：经过综合器优化后，输出端口已经不起作用了

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原因：第 9 脚，空或接地或接上了电源

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原因：是你作为时钟的引脚没有约束信息。可以对相应的做一下设定就行了主要是指你的某些管脚在电路当中起到了时钟管脚的引脚。

作用，比如触发器的 CLK 管脚，而此管脚没有时钟约束，因此 QuartusII 把“时钟”作为未定义的时钟。

措施：如果 CLK 不是时钟，可以加“时钟”的约束；如果是，可以在时钟设置当中加入；在某些对时钟要求不很高的情况下，可以忽略此警告或在这里修改：作业>定时分析设置>个人>时钟……

注意在适用于节点中只用选择时钟引脚一项即可，需要 5%即可 Fmax 一般比所要求频率高，无须太紧或太松。

6。设备 EPM570T144C5 时序特点初探

原因：因为 MAXII 是比较新的元件在 QuartusII 中的时序并不是正式版的，要等服务包

措施：只影响 Quartus 的波形

7：警告：当前设备家族支持 PLL 偏移的时钟延迟分析，但未启用

措施：将设置中的时序要求和选项-->设置-->设置更多的时间——>使时钟延迟中的改成关上

8。发现时钟的时候违反在 14.8 ns 的登记”|计数器|
lpm_counter：count1_rtl_0 | DFFS [11]”

原因：违反了设置/保持时间，应该是后仿真，看看波形设置是否和时钟沿符合设置/保持时间

措施：在中间加个寄存器可能可以解决问题

9.warning：电路可能不 operate.detected 46 非操作路径的时钟偏移大于数据延迟时钟 clk44 时钟

原因：时钟抖动大于数据延时，当时钟很快，

And if and other classes of excessive levels of this problem will occur, but this problem is mostly in the device's highest frequency will appear

Measures: setting-->timing, Requirements&Options-->Default, required, Fmax change smaller, such as change to 50MHZ

10.Design, contains, <number>, input, pin (s), that, do, not, drive, logic

Reason: the input pin does not drive logic (drive other pins), and all input pins require input logic

Measure: if this is intentional, ignore, and if unintentional, enter logical drive

11.Warning:Found, clock, high, time, violation, at, 8.9ns, on,'TEST3.CLK', node

Reason: the PLS input in FF is too short to hold

Measure: set higher clock frequency in FF

12.Warning:, Found, s, node, clock, in, paths, which, may, be, acting, ripple, and/or, gated, clocks - node (s), analyzed, as, buffer (s), resulting,, in, clock, skew, as

Reason: if you use CPLD with only one set of global clocks, another clock produced by dividing the global clock is used as a signal processing in the wiring, which cannot guarantee low clock skew (SKEW). The clock circuitry that causes work on this clock is unreliable, and even wiring problems are different.

Measure: if you have FPGA chips with more than two sets of global clocks, you can solve the problem by using second global clocks as another clock.

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14.Warning:, Can't, find, signal, in, vector, source, file, for,, input, pin, |whole|clk10m

Reason: at this point, because your file source (vector) doesn't add all the input signals (input, pin), you need an incentive source for each input

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Reason: trying to compile a file that does not exist. The file may have been renamed or deleted

Measures: no matter what he does, it doesn't matter

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The reason: the name of the module and project the name of the same name.

Measure: change one of the two names, and change the name of the module

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Reason: the module is not generated in this project, but is generated directly from the schematic and source of the other project, rather than adding the file to the project using QUARTUS. Copy

Measures: do not bother, does not affect the use

Twenty

<名称>定时装置的特点进行了初步

原因：目前版本的 QuartusII 只对该器件提供初步的时序特征分析

措施：如果坚持用目前的器件，无须理会该警告关于进一步的时序特征分析会在后续版本的 Quartus 得到完善。

21、时序分析不支持锁存器作为当前选定设备家族的同步元素的分析。

原因：用 analyze_latches_as_synchronous_elements 设置可以让 quaruts II 来分析同步锁存，但目前的器件不支持这个特性

措施：无须理会。时序分析可能将锁存器分析成回路。但并不一定分析正确。其后果可能会导致显示提醒用户：改变设计来消除锁存器，但实际其实无关紧要

22。警告：没有给输出管教指定负载电容

原因：没有给输出管教指定负载电容

解决方法：该功能用于估算 TCO 和功耗，可以不理会，也可以在编辑中为相应的输出管脚指定负载电容，以消除警告